Data Technology Corporation

DTC 500B Series
DISK CONTROLLERS

USER'S MANUAL

DATA TECHNOLOGY CORPORATION

DTC 5ØØB SERIES DISK CONTROLLERS

USER'S MANUAL

DTC part number Ø9-ØØ181. Revision ØØ

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PREFACE

Warranty

Data Technology Corporation (DTC) maintains a complete Repair Department for the sole purpose of providing efficient, reliable service. All DTC products are warranted against defects in material and workmanship. The period of coverage and other warranty details are clearly specified in the DTC purchase agreement. Check this agreement for exact warranty details.

Accuracy

All information in this manual is based on the latest product information available at the time of printing. DTC has reviewed the accuracy of the technical specifications, but DTC cannot be held responsible for any omissions or errors that may appear in this manual.

Change Information

The DTC product line is constantly being reviewed and improvements are implemented when appropriate. From time to time DTC will distribute Field Change Orders and Technical Bulletins to inform users of enhancements or improvements to their products.

Trademarks

LSI-11 is a trademark of Digital Equipment Corporation
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IBM Personal Computer is a trademark of International Business Machines Corporation.
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SECTION 1

1.1 Scope of Guide

This guide, for Data Technology Corporation's 500B Series Disk Drive Controllers, provides:

Equipment Information and Specifications
Interface and Configuration Information
Command and Programming Information
Installation and Testing Instructions
Maintenance and Troubleshooting Hints

This guide is intended to satisfy the information requirements of OEM Engineers; Engineering and Production Technicians; Personal Computer Enthusiasts; and others with a need to know about these disk Controllers.

1.2 Overview of Equipment

The DTC-510B is designed to control two industry standard ST506/406 or compatible 5.25 Winchester Disk Drives.

The DTC-520B is designed to control a maximum of four disk drives. It supports up to two ST506/406 or compatible 5.25 inch Winchester Disk Drives plus two industry standard SA4XX, or equivalent, (48 or 96TPI) Floppy Disk drives.

The DTC-535B is designed to control a maximum of four drives in any combination of up to two industry standard 5.25 inch Winchester Disk Drives, and any combination of two industry standard SA8XX type interface 8 inch Floppy Disk Drives. Alternately, it can be strapped for a combination of two hard disk drives and two AMLYN 5850 drives or one SA8XX and one AMLYN 5850.

The DTC-535BK is designed to control a maximum of four drives in any combination of up to two industry standard ST506 5.25 inch Winchester Disk Drives, or equivalent, or up to four 5.25 inch KODAK 3.3 Floppy Disk Drives.

Currently supported disk drives are produced by:

KODAK	IMI	SEAGATE	COGITO
BASF	MPI	SHUGART	QUANTUM
Cii-HB	OPE	TANDON	MICROPOLIS
CMI	RODIME	TI	TULIN
FUJITSU	MINISCRIBE	MICROSCIENCE	MAXTOR

The interface to the Host Computer is via the industry standard SASI bus and is easily accomplished by a standard DTC Host Adapter. DTC is a major supplier of SASI compatible Host Adapters for most computer system buses.

1.2 Overview of Equipment (continued)

Contact your DTC sales representative for information on available Host Adapters.

Proprietary LSI Circuits, based on DTC's field-proven design, allow for enhanced performance, small size and economy. Reliability and maintainability have been proven by statistical information from field installation. The Mean Time between Failures (MTBF) for these Controllers is 20,000 hours. The Mean Time to Repair (MTTR) is 0.1 hour.

Features found in a DTC-500B Series Controller are given in Table 1-1.

TABLE 1-1

Controller Features

AUTOMATIC SEEK VERIFY	A seek command is implied in every data transfer command (READ, WRITE, CHECK TRACK FORMAT, etc.). If the heads are not positioned over the correct cylinder, a seek is initiated, and a cylinder verification is performed after the seek completes.
MULTIPLE BLOCK TRANSFERS	Allows more than one block to be transferred with one command.
AUTOMATIC HEAD and CYLINDER SWITCHING	When the end of a track is reached (during a multi-block data transfer) the Controller switches heads to the next track. When the end of a cylinder is reached, the Controller seeks to the next cylinder, selects head 0 and resumes transfer.
PARITY SELECTION	Odd parity is generated within the Controller for all information put on the I/O bus. When parity is enabled (by jumper selection) all bad parity information is flagged.
PROGRAMMABLE SECTOR INTERLEAVING	Up to a 16 way programmable interleave is provided.
HARD DISK SECTOR SIZE	Selectable Winchester Sector size of 256 bytes (33 Sectors), 512 bytes(18 sectors), or 1,024 bytes (9 Sectors).
PROGRAMMABLE FLOPPY TRACK FORMAT	The type of track format on the floppy media that is going to be used can be passed to the Controller through software.

TABLE 1-1 Controller Features (continued)

MEDIA ASSIGNMENT FUNCTION	This function allows the user to read conventional 48 tpi or 96 tpi diskettes on KODAK 3.3 disk drive.
HOST INTERFACE PROTOCOL	A bi-directional (SASI) bus between the Controller and Host provides a simple and efficient communication path. A high level command set permits effective command initiation.
LOGICAL to PHYSICAL DRIVE CORRELATION	Logical unit numbers (LUN's) are independent of physical port numbers. All accesses specify LUN's
PROGRAMMABLE DISK DRIVE PARAMETERS	The disk drive parameters are passed to the Controller from the Host (as data) to define the drive's characteristics. Standard firmware supports up to 8 heads. Up to 1024 cylinders are supported. Optional firmware on some Controllers support up to 16 heads.
DOUBLE STEP FUNCTION	Allows the user to Read/Write 48 TPI diskettes on a 96 TPI Floppy Drive.
CONTROLLER ID SELECTABLE	A jumper is provided to specify the Controller ID number on the 510B and 520B. The 535B and 535BK use switches to specify the Controller ID number.
ON BOARD SECTOR BUFFER	A sector buffer is provided on the Controller to eliminate the possibility of data overruns during a data transfer.
ALTERNATE TRACK ADDRESSING	The Host can assign an alternate track for a defective track. (Subsequent accesses to the defective track will cause the Controller to transfer data from the alternate track address). The maximum number of alternate track addresses is half the total number of tracks on the disk.
DATA ERROR SENSING and CORRECTION	If a data error is detected during a disk data transfer, the Controller indicates whether or not it is correctable. If correctable, either a pointer and mask can be requested by the Host for applying the correction or the error can be automatically corrected.

TABLE 1-1 Controller Features (continued)

FAULT DETECTION	In the 500B series Controller, two classes of faults are flagged to improve error handling: * Controller faults * Disk faults
ERROR INDICATORS	Eight LED indicators are installed to aid in the analysis of errors.

1.3 Specifications

Specifications are given on Table 1-2.

TABLE 1-2

Specifications

Environmental Parameters	Operating	Non-Operating
Ambient Temperature	32 to 131 degrees F 0 to 55 degrees C	-40 to 167 degrees F -40 to 75 degrees C
Relative Humidity (At 40 degrees F wet bulb temperature and no condensation)	10% to 95%	10% to 95%
Altitude	0 to 10,000 ft.	0 to 15,000 ft.

Physical Dimensions	510B	520B	535B	535BK
Width (in.)	5.75	5.75	5.75	5.75
Length (in.)	8.35	10.00	10.35	10.00
Height (in.)	0.49	0.49	0.49	0.49
Weight (lbs)	1.12	2.00	2.00	2.00

NOTE: Mounting holes are identical to 5.25 inch disk drive mounting holes.

Power Requirements	510B	520B	535B	535BK
Voltage DC ±5% 50 millivolts peak-to-peak maximum ripple	+5v	+5v	+5v	+5v
Current AMPS Max.	2.2A	2.6A	2.6A	2.6A

1.4 Maintenance Philosophy

The error detection capability of these Controllers allows isolation of a fault to a defective disk drive or Controller. If the disk drive is faulty, the manufacturer's documentation should be reviewed to determine disposition.

A two level maintenance philosophy is recommended for the DTC-500B Series Controller and associated Host Adapter.

Level 1 - Replacement of the defective module at the user's site.

Level 2 - Replacement of defective component at DTC's manufacturing facility.

Section 4 of this manual provides maintenance and troubleshooting data that should be reviewed for additional information.

Contact DTC prior to returning any material.

1.5 Related Documents

Related documents include:

- Host CPU documentation
- Disk Drive Manufacturer's documentation
- Host Adapter Installation and Software Instructions

1.6 Inquiries

Contact your Data Technology Corporation Sales Representative or:

DATA TECHNOLOGY CORPORATION
2775 Northwestern Parkway
Santa Clara, CA 95051
(408) 496-0434
TWX 910-338-2044

DATA TECHNOLOGY CORPORATION
15 Wiggins Avenue
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SECTION 2

HOST AND DISK DRIVE INTERFACES

2.1 Interface Connections

Figure 2-1 is a block diagram of a typical system configuration. (See the Appendices in back of this manual for the location of the Controller's Cable and Power Connectors). The Host Computer's I/O Bus is attached to the Controller with the appropriate Host Adapter. The Host Adapter ensures signal compatibility between the Host Computer and the Controller. The Host Adapter translates the signals transferred between the Host Computer's I/O Bus and the Controller's SASI Interface. This includes directing signals, with the correct polarity, level and timing to the corresponding connector pin.

The Winchester Disk Drive Control Interface exchanges status and control information between the Controller and the Disk Drive(s).' It is daisy-chained to each Disk Drive attached to the Controller, and a terminator is installed in the last physical Disk Drive connected to the chain.

Disk Drive parameters, such as the maximum number of cylinders and number of heads, are passed to the Controller from the Host Computer. This allows Disk Drives with different parameters and characateristics to be attached concurrently to the Controller with no special requirements.

The Winchester Disk Drive's Data Interface has a separate cable for each Disk Drive. It exchanges serial MFM Data between the Controller and the Selected Disk Drive.

The Controller's D.C. Power Interface requirements are given in Table 1-2.

2.2 Host Interface

The Controller's Host Interface is attached, via the appropriate Host Adapter, to the I/O Bus of the Host Computer. Each computer manufacturer specifies the signal names and timing considerations for their I/O Bus.

Figure 2-2 shows the name, pin designation, and direction of the signals on the Controller's Host Interface connector.

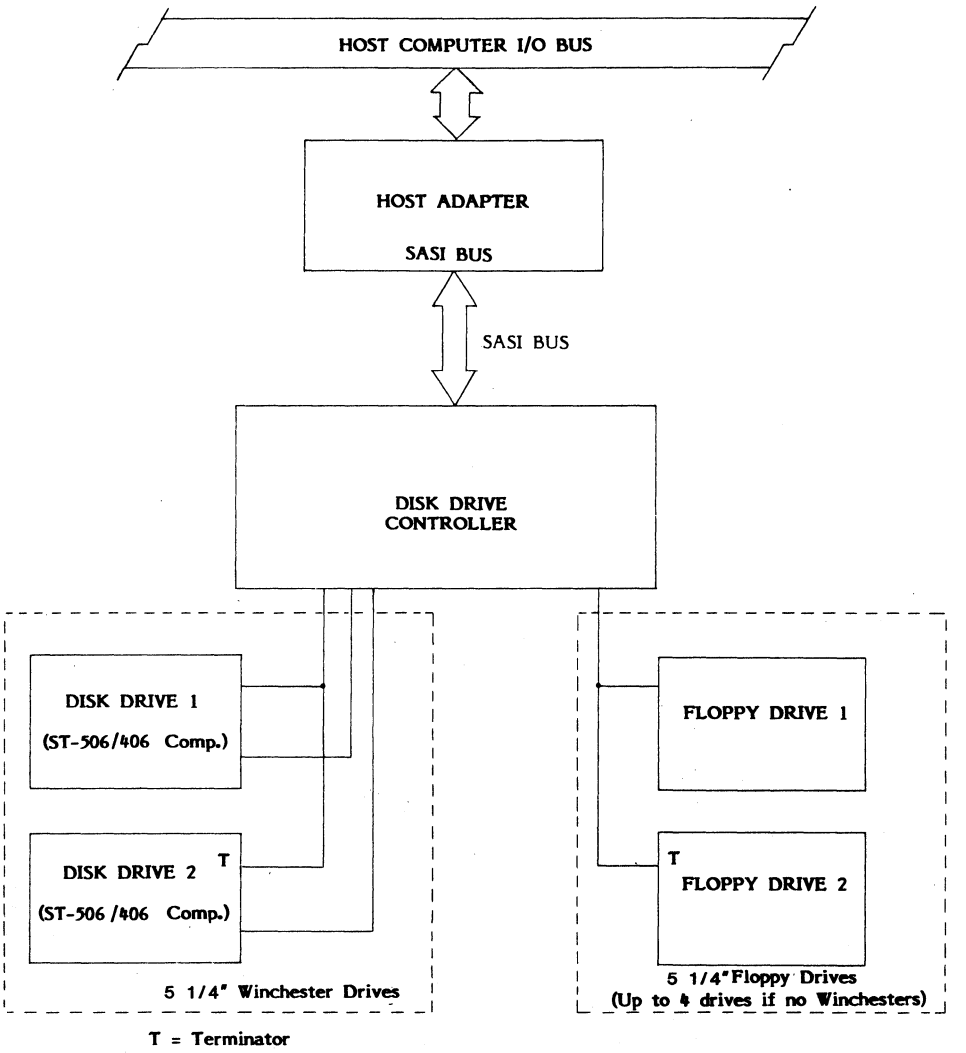
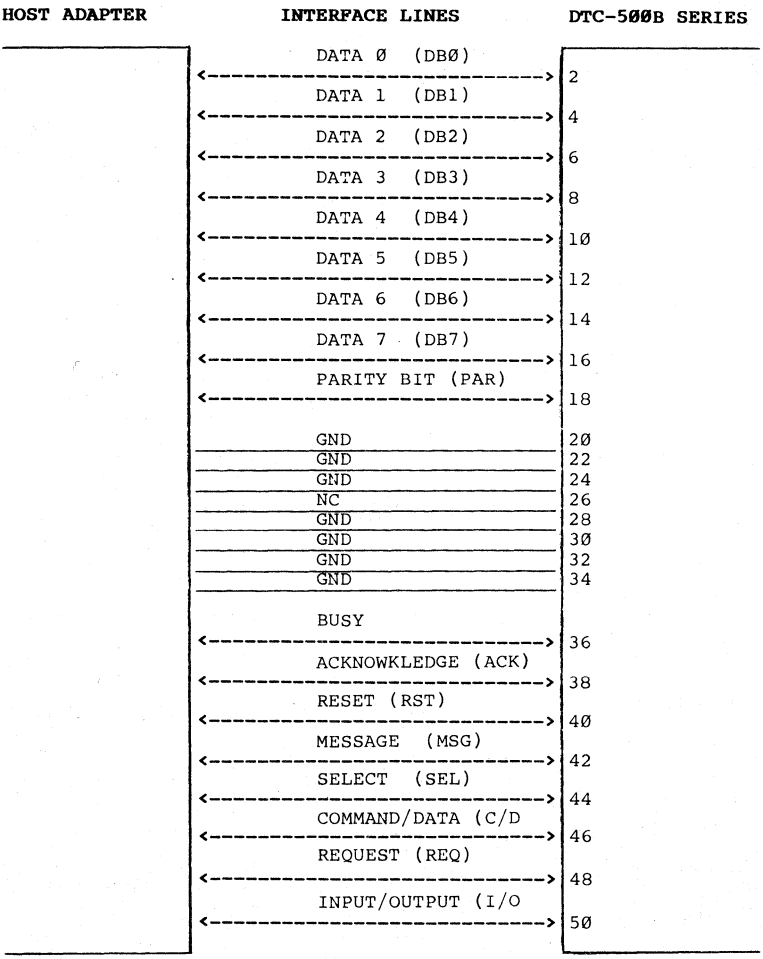


Figure 2-1 Typical System Configuration



NOTE: All signals are negative true and all odd pins are connected to ground (except for pin 25). The signal lines are terminated with 22Ø ohms to 5V and 33Ø ohms to ground. Pin 25 and 26 can be used for terminator power so they are left unconnected.

FIGURE 2-2 HOST INTERFACE SIGNALS and PIN DESIGNATION

2.2 Host Interface (continued)

The Controller's Host Interface uses negative-logic (negative or low true logic) and utilizes a bi-directional 8-bit bus with a jumper selectable parity bit. The Controller regulates transfers across the bus in a manner that permits connection to Host computers utilizing Direct Memory Access (DMA) as well as to those Host computers that support only programmed input/output transfers (the Controller also regulates data transfers across the bus to eliminate data overruns that could occur during the transfer to data).

2.3 Signal Definitions

In this manual, the term "Asserted" means that the signal on the Host Interface is true and between Ø.Ø Volts and +Ø.8 Volts. The term "Deasserted" means that the signal on the Host Interface is false and between +2.5 volts and +3.5 volts.

2.3.1 Bi-directional Bus Signals

Data Ø through Data 7 and Parity Bit - These lines represent the eight data bits and the Parity bit that is passed between the Host Computer and the Controller in the form of a command or data byte. Because the Controller utilizes odd parity,(when enabled) the number of bits asserted on this bus (by the Controller) will always be odd. The Controller will issue a parity error flag if an even number of bits are asserted on this bus by the Host Computer.

2.3.2 Uni-directional Signals from the Host Adapter

These are input signals to the Controller from the Host Adapter.

ACKNOWLEDGE (ACK)

This bit is asserted as a response to REQ from the Controller. ACK must be returned for each REQ assertion. The Controller will wait for the assertion of ACK before REQ is deasserted. The Host Adapter must not deassert ACK until after REQ has been deasserted. If the Host Adapter keeps ACK asserted, the Controller will not reassert REQ until after ACK is deasserted. This provides the Host Adapter with a means of regulating the transfer of bytes across the bus. Byte transfer regulation can occur for either command or data bytes.

2.3.2 Uni-directional Signals from the Host Adapter (continued)

RESET (RST)

When asserted, this bit will force the Controller to the beginning of its microcode program and set all drive parameters to their default value. Reset immediately terminates any pending command without the transmission of the status or message bytes. Any error status request (after RST has been asserted) will result in invalid status information being transferred. All Disk Drive interface lines are deasserted. Reset must be asserted for a minimum of 25Ø nanoseconds and a maximum of 1Ø seconds. The Controller monitors its Host Interface and waits for an asserted Select (SEL) signal and the asserted ID bit corresponding to the Controller after Reset.

SELECT (SEL)

When asserted, indicates the beginning of the command transaction. The Host Adapter asserts SEL to gain the attention of the Controller. A Data bit on the bus must also be asserted during SEL time to select a Controller. The Controller will return BUSY as acknowledgement for SEL. After the assertion of BUSY, the Host Adapter will deassert SEL and the data bit (ID bit). The Controller will wait until SEL is deasserted before it asserts REQ. SEL can be asserted immediately following a Reset.

2.3.3 Uni-directional Signals from the Controller

These are the output signals from the Controller to the Host Adapter:

Input/Output (I/O) - When asserted, the information on the bi-directional Bus is driven by the Controller. When deasserted, the information on the bi-directional Bus is driven by the Host. The Host may use this signal to enable its Data Bus line drivers.

Command/Data (C/D) - When asserted, the information bytes transmitted across the bi-directional Bus are command, status, or message bytes. When deasserted, the bytes transmitted across the bi-directional Bus are data bytes.

Busy (BUSY) - This bit is asserted in response to the Select signal and ID bit being asserted from the Host to indicate that the Controller's Host Interface is currently in use. Busy remains asserted through the message phase.

Message (MSG) - When asserted, this line indicates that the command is completed. This bit is always followed with the assertion of the Input/Output and Request signals.

Request (REQ) - This bit operates in conjunction with the Input/Output, Command/Data, and Message signals. See Table 2-1 for an interpretation of these signal lines.

TABLE 2-1

Interpretation of Request

State of Signal Lines

REQ	I/O	CD	MSG	Meaning
a	d	a	d	Get Command byte from Host Adapter
a	d	d	d	Get Data byte from Host Adapter
a	a	d	d	Send Data byte to Host Adapter
a	a	a	d	Send Status byte to Host Adapter
a	a	a	a	Send Message byte to Host Adapter

a = asserted d = deasserted

2.3.4 Controller/Disk Drive Interface Signals

Figures 2-3, 2-4, 2-5, 2-6, 2-7 and 2-8 show the name, pin designation, and direction of the signals on the Controller's drive interface.

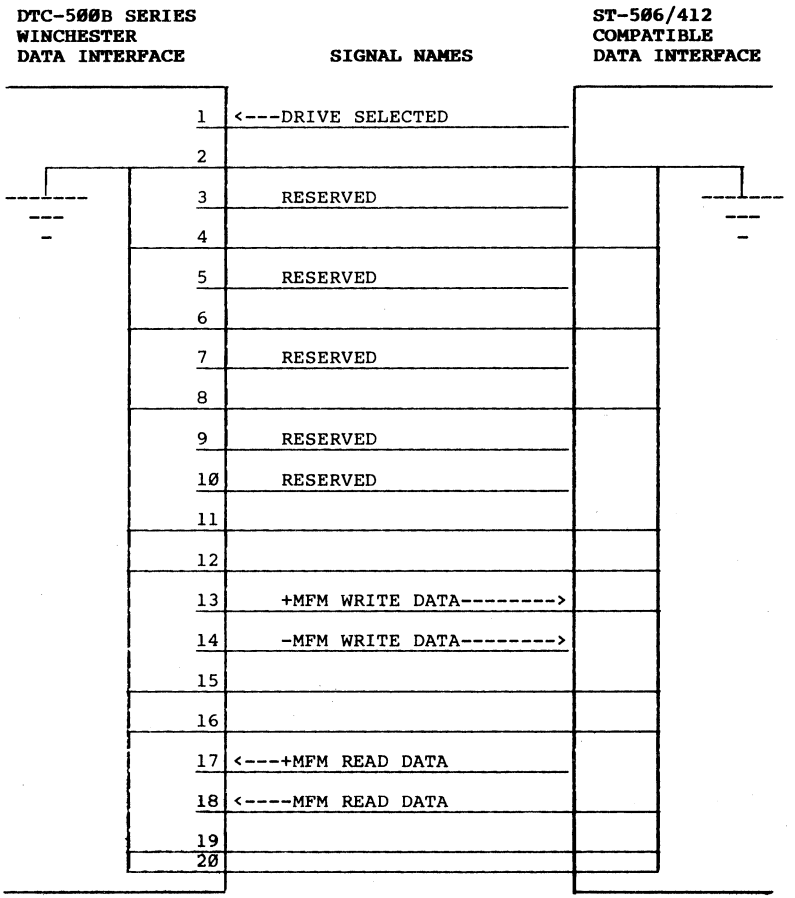
These interface signals are explained in the corresponding Disk Drive documentation.

DTC-500B SERIES WINCHESTER CONTROL INTERFACE		SIGNAL NAME		ST-506/412 COMPATIBLE CONTROL INTERFACE
	* 2	REDUCED WRITE CURRENT	--->	
	4	HEAD SELECT 2^2	--------->	
	6	WRITE GATE	--------->	
	8	<--SEEK COMPLETE		
	10	<--TRACK 00		
	12	<--WRITE FAULT		
	14	HEAD SELECT 2^0	--------->	
	16	RESERVED		
	18	HEAD SELECT 2^1	--------->	
	20	<--INDEX		
	22	<--READY		
	24	STEP	--------->	
	26	DRIVE SELECT 1	--------->	
	28	DRIVE SELECT 2	--------->	
	30	DRIVE SELECT 3	--------->	
	32	DRIVE SELECT 4	--------->	
	34	DIRECTION IN	--------->	

NOTE: All odd numbered pins are connected to signal ground.
All signals are negative true.
*See Figure 2-4 for Drive's Data Interface information

* When using Controller with optional firmware and utilizing more than eight (8) heads, this line is used as a head select line.

FIGURE 2-3 CONTROLLER to WINCHESTER DRIVE CONTROL INTERFACE



NOTE: Reserved lines may be spares.
See Figure 2-3 for Drive's Control Interface information

FIGURE 2-4 CONTROLLER to WINCHESTER DRIVE DATA INTERFACE

DTC-520B SERIES FLOPPY DISK DRIVE INTERFACE	SIGNAL NAME	5.25" FLOPPY DRIVE SA4XX COMPATIBLE
2	SPARE	
4	IN USE/SPARE	
6	DRIVE 4 SELECT----->	
8	<------INDEX	
10	DRIVE 1 SELECT----->	
12	DRIVE 2 SELECT----->	
14	DRIVE 3 SELECT----->	
16	MOTOR ON---------->	
18	DIRECTION---------->	
20	STEP---------->	
22	WRITE DATA--------->	
24	WRITE GATE--------->	
26	<------TRACK 000	
28	<------WRITE PROTECT	
30	<-----READ DATA AND CLOCKS	
32	SIDE SELECT------->	
34	SPARE	

NOTE: All odd numbered pins are connected to signal ground.
All signals are negative true.

FIGURE 2-5 CONTROLLER to FLOPPY DISK DRIVE INTERFACE (520B)

535B CONTROLLER		SA8XX INTERFACE
	EXTERNAL WRITE CURRENT SWITCHING---->	2
	<----TRUE READY *	8
	<----TWO SIDED * +	10
	<----DISK CHANGE *	12
	SIDE SELECT * + ---------->	14
	IN USE * ---------->	16
	MOTOR ON * (HEAD LOAD)---------->	18
	<----INDEX	20
	<----READY	22
	<----SECTOR	24
	DRIVE SELECT 1 (SIDE SELECT OPT)+ --->	26
	DRIVE SELECT 2 (SIDE SELECT OPT)+ --->	28
	DRIVE SELECT 3 (SIDE SELECT OPT)+ --->	30
	DRIVE SELECT 4 (SIDE SELECT OPT)+ --->	32
	DIRECTION SELECT (SIDE SELECT OPT)+-->	34
	STEP---------->	36
	WRITE DATA ---------->	38
	WRITE GATE---------->	40
	<----TRACK 00	42
	<----WRITE PROJECT	44
	<----READ DATA	46
	<----SEP DATA	48
	<----SEP CLOCK	50

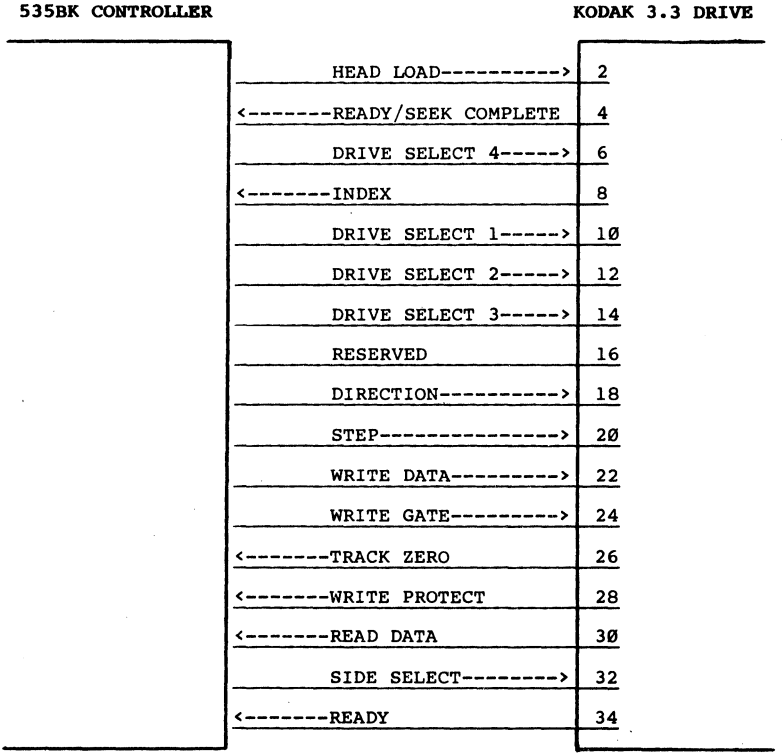
NOTE: All odd numbered pins are connected to signal ground.
All signals are negative true.
* Jumper enabled alternate I/D lines. + SA860 only.

FIGURE 2-6 CONTROLLER to FLOPPPY DISK DRIVE INTERFACE(535B)

535B CONTROLLER		AMLYN INTERFACE
	<----TWO SIDED	10
	<----DOOR OPEN	12
	SIDE SELECT ---------->	14
	NOT BUSY ---------->	16
	HEAD LOAD ---------->	18
	<----INDEX	20
	<----READY	22
	<----DISK SELECT 4	24
	DISK SELECT 0 ---------->	26
	DISK SELECT 1 ---------->	28
	DISK SELECT 2 ---------->	30
	DISK SELECT 3 ---------->	32
	DIRECTION SELECT ---------->	34
	STEP---------->	36
	WRITE DATA ---------->	38
	WRITE GATE---------->	40
	<----TRACK 00	42
	<----WRITE PROJECT	44
	<----READ DATA	46
	<----FAULT	48
	<----FAULT RESET/EJECT/RECALIBRATE	50

NOTE: All odd numbered pins are connected to signal ground.
All signals are negative true.

FIGURE 2-7 CONTROLLER to AMLYN DRIVE INTERFACE (535B)



NOTE: All odd numbered pins are connected to signal ground.
All signals are negative true.

FIGURE 2-8 CONTROLLER to KODAK 3.3 DISK DRIVE INTERFACE(535BK)

2.4 Sequence of Operation

The Controller performs an internal RAM test upon power-up. If there is a RAM failure, the Controller will display an error code 18 (hex) and will not respond to the Host.

Commands are issued to the DTC-5ØØB Series Controller via the Host Adapter following a defined protocol (SASI). The Host initiates a command sequence by selecting the Controller on the bus. If the Controller is not busy, it requests command bytes from the Host for task execution. (Command structure is described in Section 3.Ø). Upon reception of the last command byte, the Controller begins execution of the command.

For the data transfer commands, a check is performed on the disk address and status is flagged if it exceeds the drive limits. The data is stored in a sector buffer before any transfer to the Host or disk drive takes place. This buffer eliminates any possibility of data overruns between the Host and the disk.

Upon completion of the command, the Controller will send the completion status and the message byte to the Host. If an error is indicated, further delineation of the completion status may be requested by the Host issuing the appropriate sense commands. Request Sense Command will clear the error in the LED's.

Parity must be enabled or disabled on both the Host and Controller. If parity is enabled, the Controller will generate ODD parity for all data it puts on the Host Bus and it will check for ODD parity for all data it receives from the Host Bus. If parity is disabled, the Controller does not generate or check parity.

2.4.1 Select Phase

Following a Reset, and/or upon completion of a command, the Controller monitors the bi-directional Bus for the assertion of Select. The Host Adapter asserts SEL and the Controller's Address Bit on the bi-directional Data Bus to indicate that a command is ready for the Controller. The Host then waits for the Controller to respond with BUSY. Upon reception of BUSY, the Host deasserts Select and the Controller's Address Bit. The Controller now has control of the bi-directional bus.

NOTE: The Host may keep Select and the Controller's Address Bit asserted until it is ready to enter the Command Fetch Phase.

2.4.2 Command Phase

After the Host deasserts Select and the Controller's Address Bit, the Controller asserts the Command/Data (C/D) bit to indicate a Command transfer, and deasserts I/O to indicate an output from the Host. The command bytes are transferred over the bi-directional bus one byte with each REQ/ACK handshake protocol, until all command bytes are transferred to the Controller. The Command Phase ends after the last REQ pulse from the Controller is deasserted.

NOTE: The Host must not assert ACK until after REQ is asserted and must not deassert ACK until after REQ is deasserted. The Controller waits until ACK from the previous byte transfer is deasserted before it reasserts REQ to transfer the next byte. This provides a means for the Host to regulate the byte transfer across the bi-directional bus.

2.4.3 Data Phase

This phase is skipped when the command does not require a transfer of data. If a Read or Write data transfer is required for the command, the following occurs:

a. The Controller deasserts the Command/Data (C/D) line to indicate a Data transfer.

b. Depending on the command type (read or write) the I/O line (for the bi-directional bus) is asserted or deasserted by the Controller.

c. The data is transferred (one byte at a time) with the same REQ/ACK handshake protocol used in the Command Phase.

d. After all data bytes are transferred, the Controller exits this phase and enters the Status phase.

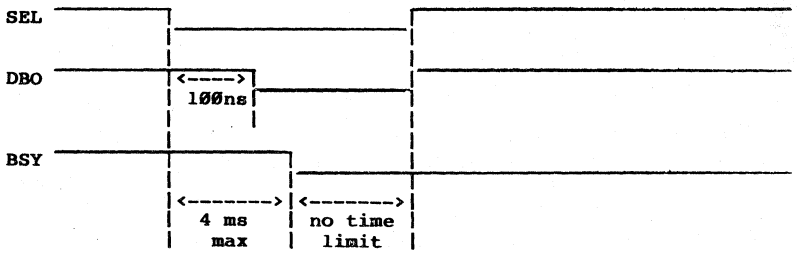
2.4.4 Status and Message Phase

After all the Command and Data bytes have been transferred, a Status byte is placed on the bi-directional bus by the Controller. (REQ,C/D, and I/O are asserted, MSG is deasserted). The Controller waits for ACK from the Host. Upon receipt of ACK, the status byte is transferred. The Controller asserts REQ, C/D, I/O and MSG to indicate to the Host that the command is complete. This action can be used to generate an interrupt in the Host. After the Host responds with ACK, the Controller will deassert BUSY, REQ, C/D, I/O, and MSG.

This completes the normal command sequence and the Controller is ready to be Selected by the Host Adapter for the next command sequence.

TIMING DIAGRAMS

Timing Requirements for Controller Selection



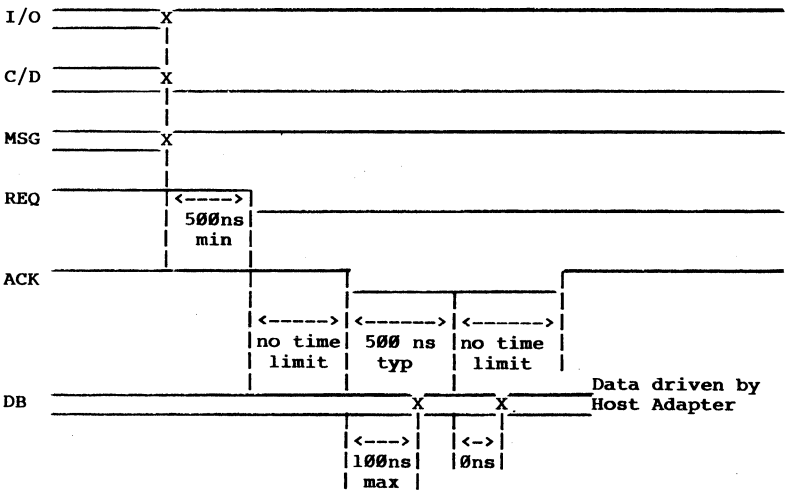
NOTES:

1. SEL must be deasserted before the Controller will assert REQ.

2. After Power On or Reset, when the first command is issued, it may take the Controller a maximum of 4 ms to respond with BUSY. The BUSY response time for all successive commands will be within 50 us.

FIGURE 2-9 TIMING DIAGRAMS (sheet 1 of 6)

Timing Requirements for Command Transfer Phase
(from Host Adapter, one byte)



NOTES:

1. I/O*, C/D*, MSG* changes 500 ns min before the 1st REQ for the phase and remain unchanged until the Controller goes into the next phase.

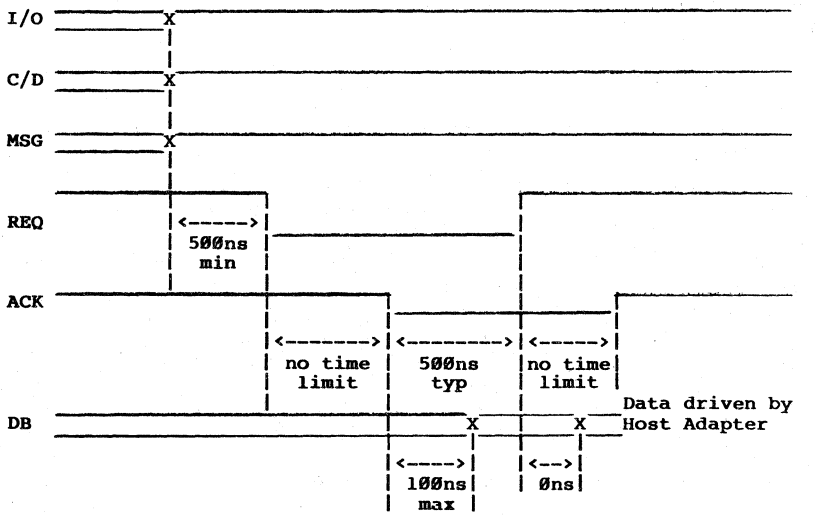
2. Data driven by the Controller is stable 100ns min at the Host Adapter end before REQ* is asserted and 0ns min after REQ* is deasserted.

3. Data driven by the Host Adapter is stable 100ns max (at the Host Adapter end) after ACK* is asserted and 0ns min after REQ* is deasserted.

FIGURE 2-9 TIMING DIAGRAMS (sheet 2 of 6)

TIMING DIAGRAMS

Timing Requirements for Data Transfer Phase
(from Host Adapter, one byte)



NOTES:

1. I/O*, C/D*, MSG* changes 500 ns min before the 1st REQ for the phase and remain unchanged until the Controller goes into the next phase.

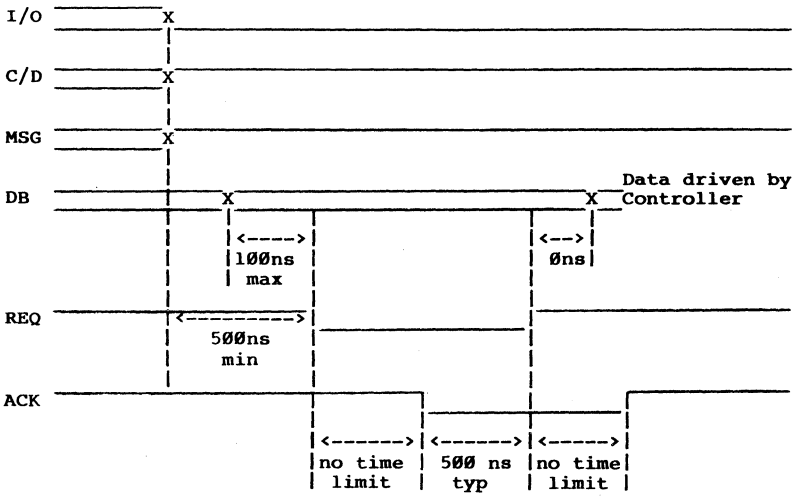
2. Data driven by the Controller is stable 100ns min at the Host Adapter end before REQ* is asserted and 0ns min after REQ* is deasserted.

3. Data driven by the Host Adapter is stable 100ns max (at the Host Adapter end) after ACK* is asserted and 0ns min after REQ* is deasserted.

FIGURE 2-9 TIMING DIAGRAMS (sheet 3 of 6)

TIMING DIAGRAMS

Timing Requirements for Data Transfer Phase (to Host Adapter, one byte)



NOTES:

1. I/O*, C/D*, MSG* changes 500 ns min before the 1st REQ for the phase and remain unchanged until the Controller goes into the next phase.

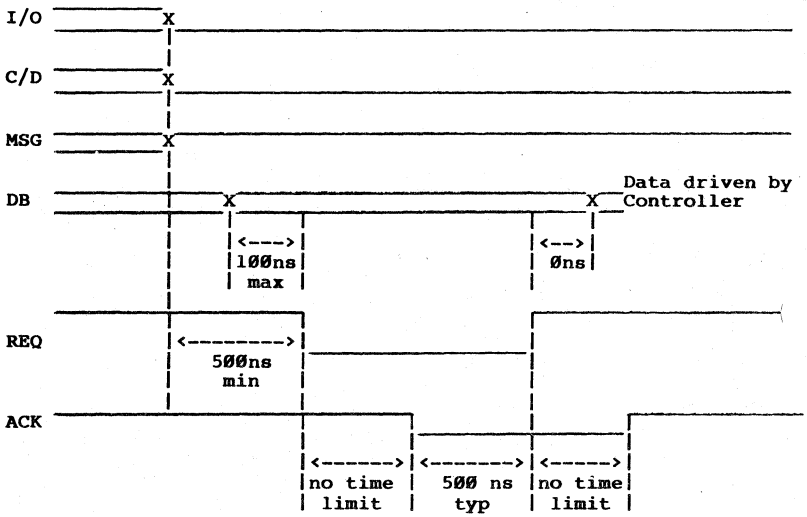
2. Data driven by the Controller is stable 100ns min at the Host Adapter end before REQ* is asserted and 0ns min after REQ* is deasserted.

3. Data driven by the Host Adapter is stable 100ns max (at the Host Adapter end) after ACK* is asserted and 0ns min after REQ* is deasserted.

FIGURE 2-9 TIMING DIAGRAMS (sheet 4 of 6)

TIMING DIAGRAMS

Timing Requirements for Status Transfer Phase
(to Host Adapter, one byte)



NOTES:

1. I/O*, C/D*, MSG* changes 500 ns min before the 1st REQ for the phase and remain unchanged until the Controller goes into the next phase.

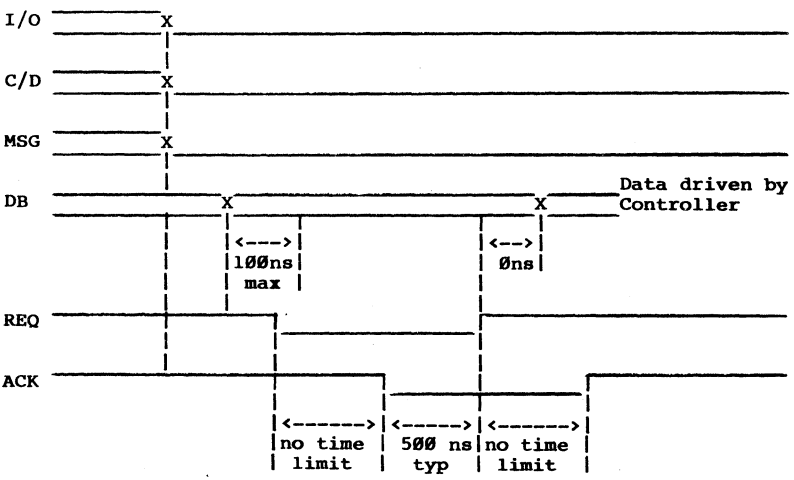
2. Data driven by the Controller is stable 100ns min at the Host Adapter end before REQ* is asserted and Øns min after REQ* is deasserted.

3. Data driven by the Host Adapter is stable 100ns max (at the Host Adapter end) after ACK* is asserted and Øns min after REQ* is deasserted.

FIGURE 2-9 TIMING DIAGRAMS (sheet 5 of 6)

TIMING DIAGRAMS

Timing Requirements for MSG Transfer
(to Host Adapter, one byte)



NOTES:

1. I/O*, C/D*, MSG* changes 500 ns min before the 1st REQ for the phase and remain unchanged until the Controller goes into the next phase.

2. Data driven by the Controller is stable 100ns min at the Host Adapter end before REQ* is asserted and 0ns min after REQ* is deasserted.

3. Data driven by the Host Adapter is stable 100ns max (at the Host Adapter end) after ACK* is asserted and 0ns min after REQ* is deasserted.

FIGURE 2-9 TIMING DIAGRAMS (sheet 6 of 6)

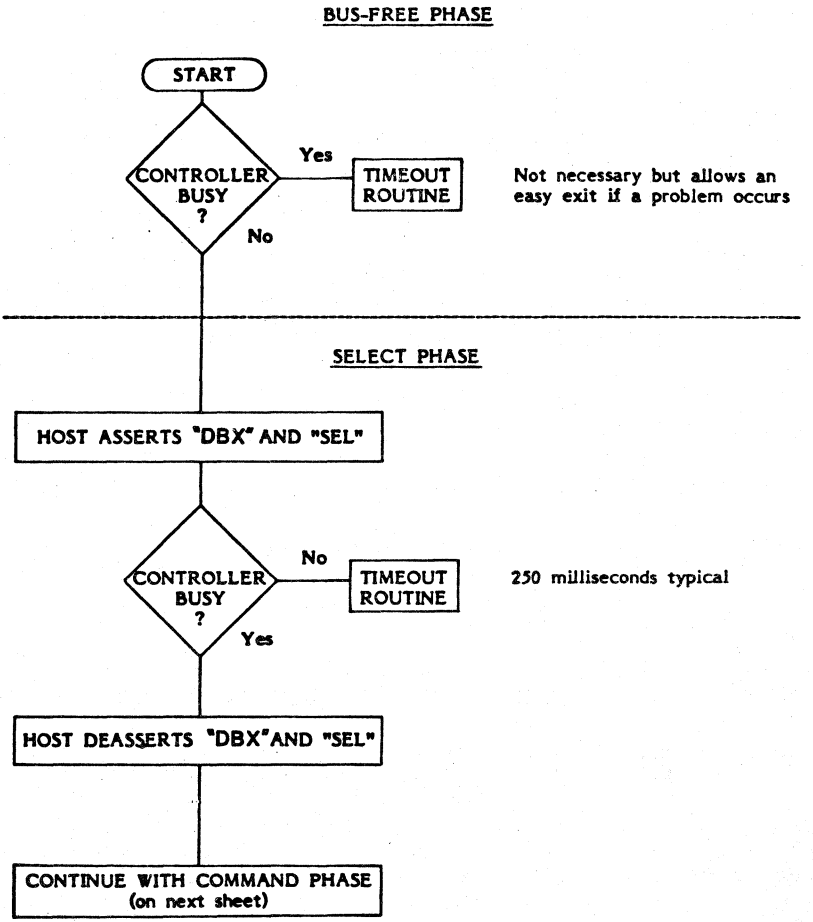


Figure 2-10 Bus-Free Phase Flowchart
(Sheet 1 of 4)

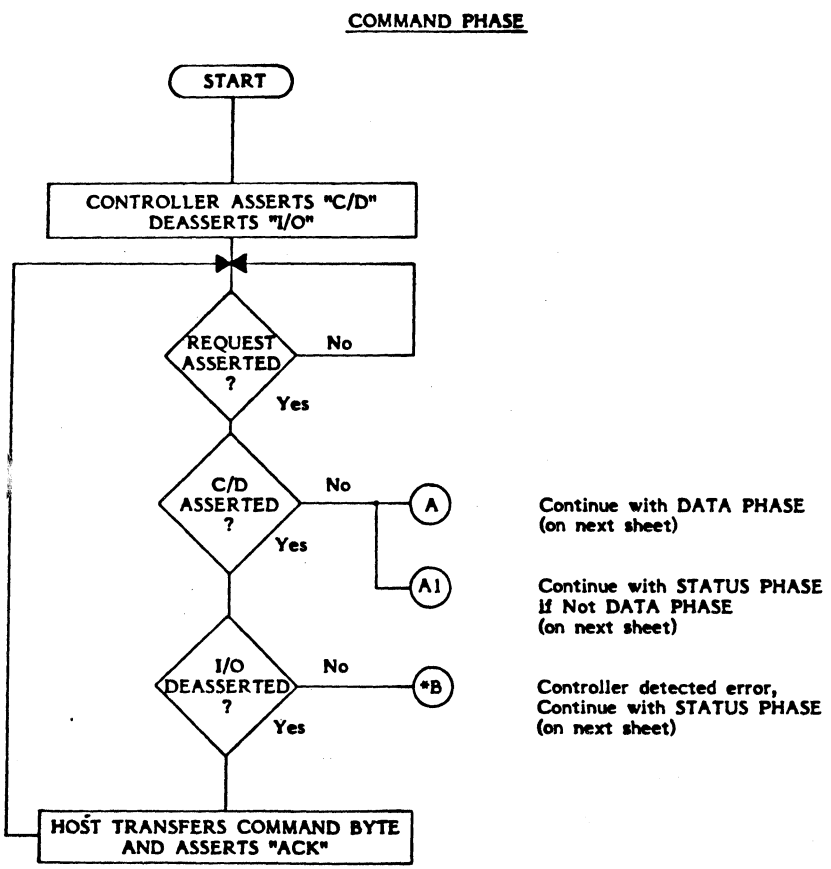
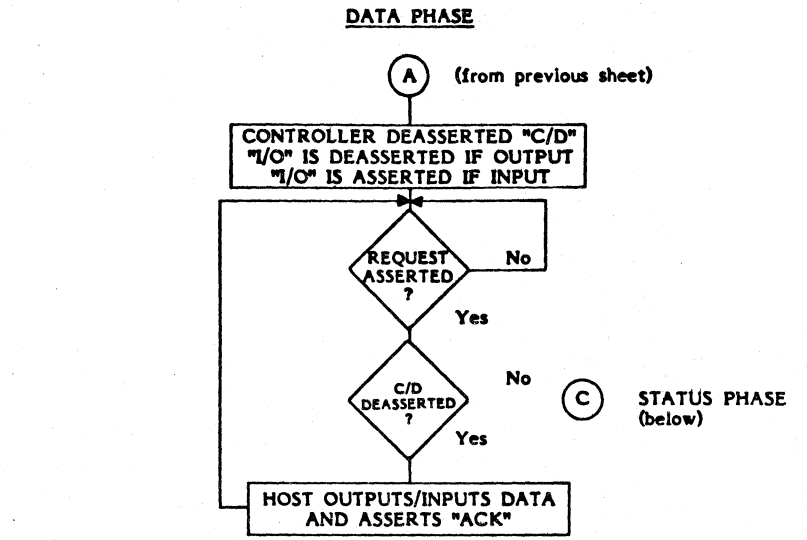


Figure 2-1Ø Command Phase Flowchart
(Sheet 2 of 4)



STATUS PHASE

* If Status Phase is entered at (*B), the Controller detected an Error condition and a Command Class Code 0, OpCode 3 (Request Sense) may be executed upon termination of the present command.

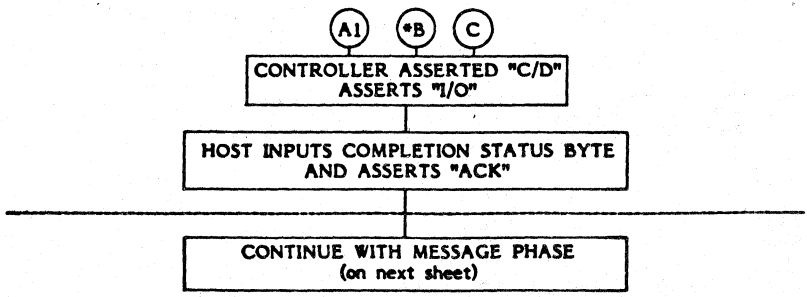


Figure 2-10 Data Phase Flowchart
(Sheet 3 of 4)

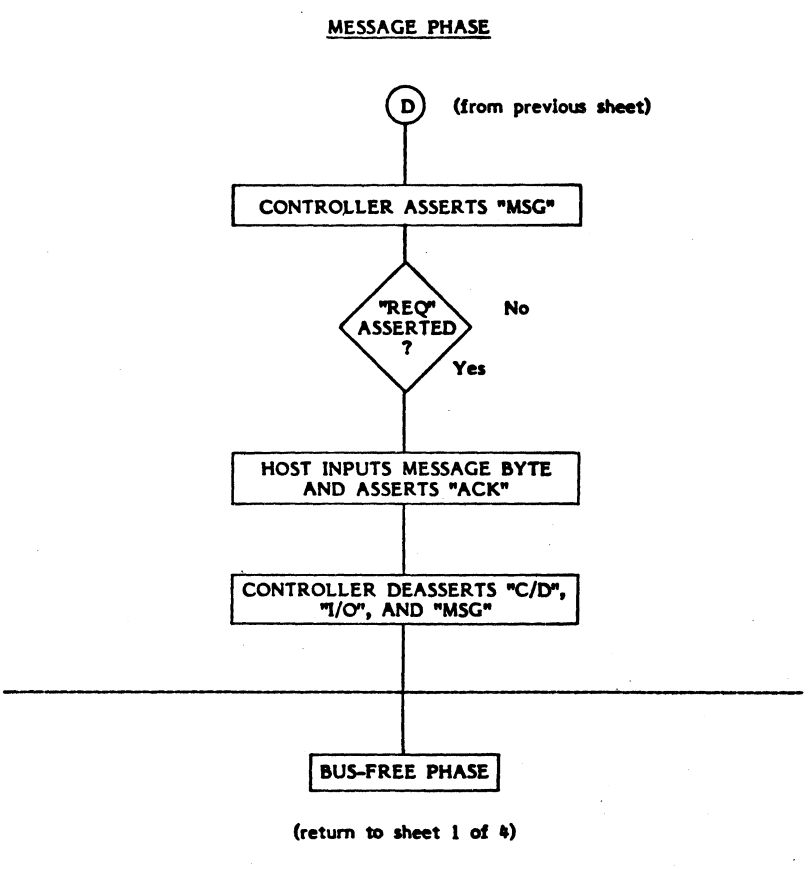


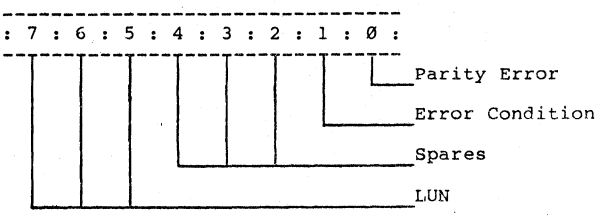
Figure 2-10 Message Phase Flowchart
(Sheet 4 of 4)

2.5 Abnormal Sequence Termination

If an error occurs, the Controller will terminate the command and will enter the Status and Message phase.

Command Completion Status

The Command Completion Status byte, as shown below, will inform the Host of any error conditions that may have occurred during the execution of the Command. This byte is returned to the Host after every command.



LUN is the Logical Unit Number of the Drive.

Bits 4, 3 and 2 are spares, set to Ø.

Error Condition indicates that an error, other than a parity error, has occurred.

Parity Error is indicated separately by bit Ø.

Additional information on the Error Condition (bit 1) is provided to the Host with the four Sense Bytes (sent after a Request Sense Command (Class Code ØØ, OpCode Ø3). The Host can read these bytes after an error has occurred (or ignore the error condition). The Sense Bytes are explained in Paragraph 3.2.4.

Command Completion Status (continued)

Error conditions are classified as follows:

1. Bi-directional Bus Parity Errors - Upon detection of a Parity Error in a command or data transfer from the Host, the Controller completes the current phase and enters the Status and Message phase. The Status byte indicates a Parity Error has occurred.

2. Drive Interface or Controller Related Errors - An error of this type can be detected after the Command bytes have been accepted. Upon detection of this error condition (which could be caused by a Drive Fault, Drive Not Ready, or Illegal Command), the Controller will enter the Status and Message phase. The Status byte sets the corresponding error bits.

3. Read/Write Channel Errors - The Controller may transfer a sector, or more, of data before it detects this type of error and upon detection of this type of error (Read data error, Record not found, Drive Fault during a write), the corresponding error bits are set in the status byte.

In cases 2 and 3, the Host may issue a Request Sense command and retrieve additional error information as explained in Paragraph 3.2.4.

NOTE: An error condition will not inhibit the Host from issuing another command.

SECTION 3

COMMANDS AND STATUS

3.1 Overview

The Host issues a command to the Controller by passing it a CDB (Command Descriptor Block). Figure 3-1 shows the format of a typical Class Code Ø CDB. Byte Ø is the first byte sent to the Controller.

	MSB						LSB
BYTE #	7	6	5	4	3	2	1 Ø
Ø	CLASS CODE			OPCODE			
1	LUN			LOGICAL ADDRESS 2			
2	LOGICAL ADDRESS 1						
3	LOGICAL ADDRESS Ø						
4	See Paragraph 3.1						
5	See Paragraph 3.1						

LUN = Logical Unit Number

Figure 3-1

Typical Command Descriptor Block (CDB)

Byte Ø of the CDB contains a 3-bit Class Code and a 5-bit Opcode. **The significance of Byte Ø is the same in every CDB.**

The 3-bit Class Code allows up to eight different Class Codes.

- Class Ø (ØØØ) - Used for non-data or data transfers and for Status Command transfers.
- Class 1 (ØØ1) - Used for the Disk Copy Command.
- Class 5 (ØØØ) - Supercopy command and DTC extended commands (51ØB only).
- Class 6 (11Ø) - Used for transferring programmable parameters of a disk drive from the Host to the Controller.
- Class 7 (111) - Used for diagnostic commands.
- Class 2 through 5 are reserved on the 52ØB, 535B, and 535BK.
- Class 2 through 4 are reserved on the 51ØB.

Typical Command Descriptor Block (CDB) (continued)

The 5-bit Opcodes are described within the description of each Class Code.

Byte 1 of the CDB contains a 3-bit LUN (Logical Unit Number) and the five most significant bits of the Logical Address (Logical Address 2). The LUN is contained in every CDB. It corresponds to the Drive Select jumper on the drive.

Example:

Winchester Drive Select 1 = LUN Ø
Winchester Drive Select 2 = LUN 1
Floppy Drive Select 3 = LUN 2
Floppy Drive Select 4 = LUN 3

On the 535B, when using two AMLYN drives, LUN 2 will represent diskettes 1-5, LUN 3 will represent diskettes 6-1Ø. A switch on the AMLYN drive will determine the LUN. The Media Select Command will select the desided diskette.

On the 535B,if one AMLYN and one 8 inch floppy are to be used, the AMLYN drive must be LUN 2 and the 8 inch floppy must be LUN 3.

For copy commands:

SLUN = Source drive LUN.
DLUN = Destination drive LUN.

Logical Address is a 21-bit address. It is comprised of 5 bits from byte 1, 8 bits from byte 2, and 8 bits from byte 3. With the use of Logical Address, a unique address (which corresponds to the Logical Address value) is assigned to each individual sector within a disk drive by the Controller.

To better understand the Logical Address concept, view the sectors of any disk drive as sequentially numbered - starting with Ø (at track Ø, sector Ø) and ending (with the accumulated total of all sectors) at the last sector, of the last track, of the last disk surface. The Logical Address is explained in more detail in Appendix A.

Byte 2 contains 8-bits of the Logical Address (Logical Address 1).

Byte 3 contains the eight least significant bits of the Logical Address (Logical Address Ø).

The significance of Byte 4 and Byte 5 (in the CDB) depends on the CDB's Class Code and OpCode (Byte Ø of the CDB). Bytes 4 and 5 are explained, when significant, within the OpCode descriptions.

3.2 Class Code Ø Commands

Class Code Ø OpCodes are summarized in Table 3-1. Paragraphs 3.2.1 through 3.2.13 provide additional information on each OpCode.

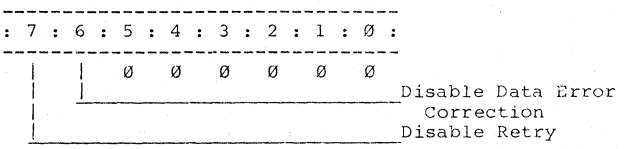
Class Code Ø Command Byte Ø through 3 of the CDB are as shown earlier in Figure 3-1 and as described in Paragraph 3.1.

Byte 4 of the Class Code Ø CDB contains the number of blocks (Sectors) to be transferred with each OpCode Ø8 (Read) and ØA (Write) commands. A Ø value, in Byte 4, will cause a transfer of 256 sectors.

Byte 4 also indicates the interleave factor for OpCodes Ø4 (Format Drive), Ø6 (Format Track), Ø7 (Format Bad Track), Ø5 (Check Track Format), and ØE (Assign Alternate Track). Appendix B provides additional information on interleave computations.
NOTE: Interleave values of Ø to 1 result in the identical track format.

Byte 5 of the Class Code Ø CDB is the Control byte used with OpCodes Ø8 (Read), ØA (Write) and ØE (Assign Alternate Track). This byte contains the control bits that tell the Controller how to react if an error condition is encountered during the Data phase of the command.

Byte 5 is defined as follows:



Disable Retry (Bit 7):

If this bit is set, the Controller will not attempt to retry the command upon certain error conditions where retry could be attempted.

If this bit is not set, a total of eight retries will be performed before an error is reported.

If retry is successful, the Controller will not report the error to the Host. The following errors may result in a retry attempt:
(a) Record not found during Read or Write command.
(b) Seek error during Read or Write command.
(c) Correctable or uncorrectable data error during Read command.

For error conditions (a) and (b), a Recalibrate Seek and Read are performed.

For error condition (c), only reread is performed.

NOTE: No retry is performed if the Check Track command encounters the No ID address mark error.

3.2 **Class Code Ø Commands** (continued)

Disable Data Error Correction (Bit 6):

If this bit is set, the Controller will not correct the data that is read from the disk if an ECC error occurred during a read.

If this bit is not set, data errors will always be corrected, (if correctable) before being transferred to the Host.

The information returned by the Request Sense command will indicate whether or not the data error is correctable.

Regardless of the error condition, the data is transferred to the Host.

TABLE 3-1

Summary of Class Code Ø OpCode

Opcode (Hex)	Class Code Ø Command Description
ØØ	**TEST DRIVE READY.** Selects the drive and verifies that the drive is Ready and that a seek is not in progress
Ø1	**RECALIBRATE.** Positions the Read/Write heads at TrackØØ, clears drive's error status.
Ø2	**REQUEST ECC SYNDROME.** Returns four bytes of offset and syndrome for data field error correction. The four bytes are returned as Data (C/D deasserted) with the following format:

	MSB							LSB
BYTE #	7	6	5	4	3	2	1	Ø
Ø	M.S. BIT OFFSET (8)							
1	L.S. BIT OFFSET (8)							
2	Ø							
3				MASK (4BITS)				

The bit offset is relative from bit Ø of Byte Ø. To obtain the valid syndrome, this command must be issued immediately after the correctable data error.

TABLE 3-1

Summary of Class Code Ø OpCodes (continued)

Opcode (Hex)	Class Code Ø Command Description
Ø3	**REQUEST SENSE.** This command must be issued immediately after an error. It returns 4 bytes of drive and Controller sense information as data (C/D deasserted) for the specified LUN (see paragraph 3.2.4 for details and exceptions).
Ø4	**FORMAT DRIVE.** Formats all blocks with ID field and data field according to the interleave factor. The data field contains E5 Hex. (Sector Formats are described in Appendix C)
Ø5	**CHECK TRACK FORMAT.** Checks format on the specified track for correct ID and interleave. Does not read the data field.
Ø6	**FORMAT TRACK.** Formats a specified track and writes E5 Hex in the data fields.
Ø7	**FORMAT BAD TRACK** (bad block flag). Formats a specified track with the bad block flag set in the ID fields of all blocks of that track. Writes E5 Hex in the data fields.
Ø8	**READ.** Reads the specified number of blocks given in Byte 4 of the CDB starting from the initial block address given by the Logical Address bytes of the CDB.
ØA	**WRITE.** Writes the specified number of blocks given in Byte 4 of the CDB starting from the initial block address given by the Logical Address bytes of the CDB.
ØB	**SEEK.** Initiates a seek to the specified block and (for those drives capable of overlap seek), immediately returns completion status before the seek is complete.
ØD	**SET INTERLEAVE** (KODAK 3.3 only). This allows the Controller to run at an optimum performance speed when used with variable Host System speeds.

TABLE 3-1

Summary of Class Code Ø OpCodes (continued)

OpCode (Hex)	Class Code Ø Command Description

ØE **ASSIGN ALTERNATE DISK TRACK.** This command is used to assign an alternate track address to a specified track. Any access to a sector in the specified track will cause the Controller to automatically access the sector at the alternate track.

This command sets the "Alternate Track Assigned" flag in the ID field of all sectors and writes the Alternate Track Address in the data field of the sectors.

The Controller then formats the alternate track. The "Alternate Track" flag is set in the sector ID fields and all data fields are written with E5 Hex. The alternate track address (four bytes) is passed to the Controller as Data (C/D deasserted). This alternate track address transfer is as follows:

	MSB							LSB
BYTE #	7	6	5	4	3	2	1	Ø
Ø	Ø	Ø	Ø	LOGICAL ADDRESS 2				
1	LOGICAL ADDRESS 1							
2	LOGICAL ADDRESS 2							
3	SPARE SET TO Ø							

NOTE: The alternate track must not have another alternate assigned to it. Refer to Appendix D for further information.

19 **MEDIA SELECT.** (for AMLYN 535B only). This allows the Controller to select the desired diskette housed in the AMLYN drive.

3.2.1 OpCode ØØ (Test Drive Ready)

This command selects the specified drive and verifies that the drive is Ready for access, i.e. Ready to accept a command.

The required fields for this command are: OPCODE and LUN.

	MSB						LSB
BYTE #	7	6	5	4	3	2	1	Ø
Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø
1	LUN					Ø		
2	Ø							
3	Ø							
4	Ø							
5	Ø							

See the flowchart in Figure 3-2 for additional information.

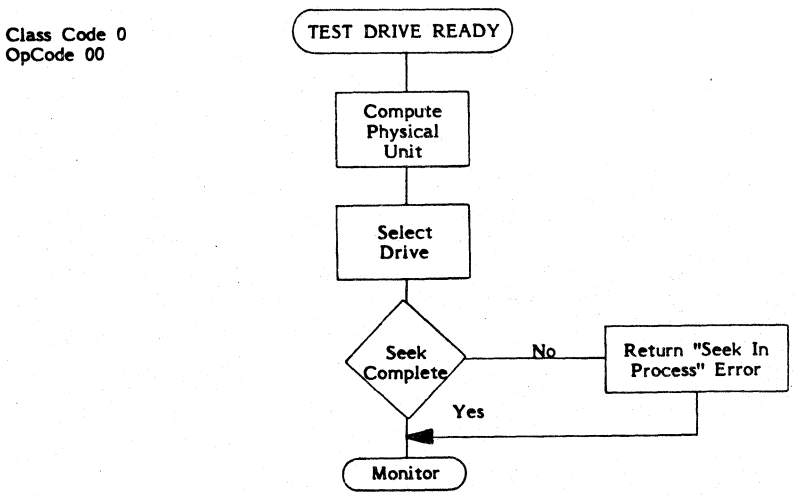


Figure 3-2 Test Drive Ready

3.2.2 OpCode Ø1 (Recalibrate)

This command positions the Read/Write heads of the selected drive to Track ØØ and clears any error status conditions from the drive.

The required fields for this command are: OPCODE and LUN.

	MSB							LSB
BYTE #	7	6	5	4	3	2	1	Ø
Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1
1	LUN					Ø		
2	Ø							
3	Ø							
4	Ø							
5	Ø							

See the flowchart in Figure 3-3 for additional information.

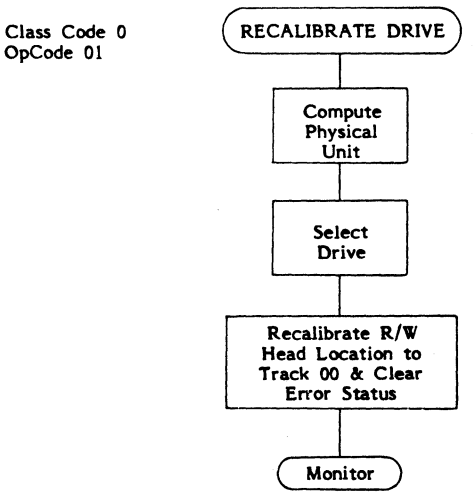


Figure 3-3 Recalibrate Drive

3.2.3 OpCode Ø2 (Request ECC Syndrome) (Not valid for floppy)

This command sends four bytes of offset and ECC data to the Host. These bytes are returned as Data (C/D deasserted). The format of these bytes is shown in Table 3-1.

The required fields for this command are: OPCODE and LUN.

	MSB						LSB
BYTE #	7	6	5	4	3	2	1	Ø
Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	Ø
1	LUN					Ø		
2	Ø							
3	Ø							
4	Ø							
5	Ø							

See the flowchart in Figure 3-4 for additional information.

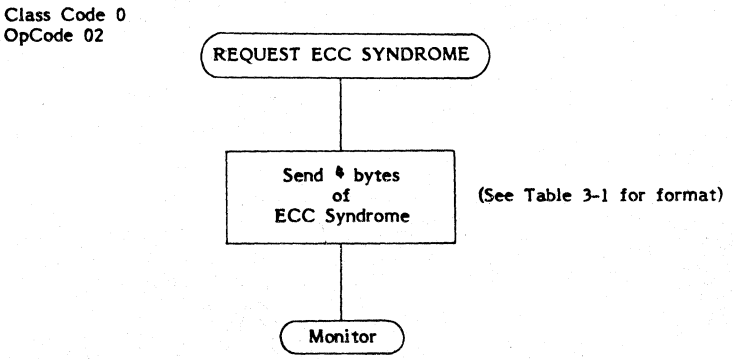


Figure 3-4 Request ECC Syndrome

3.2.4 OpCode Ø3 (Request Sense)

This command sends four bytes of error and address data to the Host. These bytes are returned as Data (C/D deasserted). The format of these bytes is shown after Figure 3-5.

The required fields for this command are: OPCODE and LUN.

	MSB							LSB
BYTE #	7	6	5	4	3	2	1	Ø
Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	1
1	LUN					Ø		
2	Ø							
3	Ø							
4	Ø							
5	Ø							

See the flowchart in Figure 3-5 and the following text for additional information.

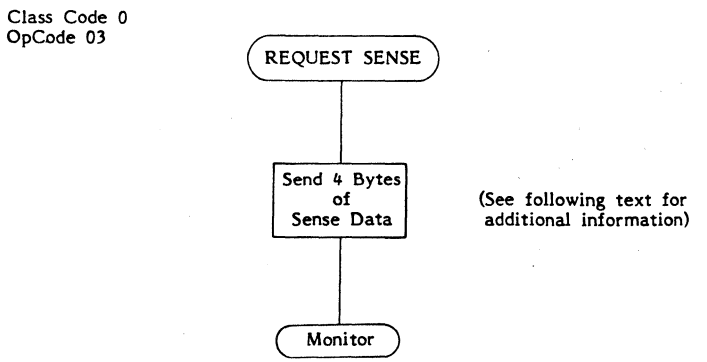


Figure 3-5 Request Sense

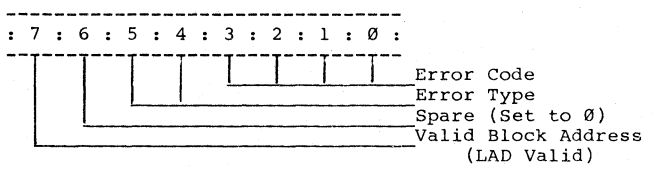
3.2.4 OpCode Ø3 (Request Sense) (continued)

The four bytes (containing Error Status, Logical Unit Number, and Logical Address) are returned to the Host in the following format:

	MSB							LSB
BYTE #	7	6	5	4	3	2	1	Ø
Ø	SENSE BYTE							
1	LUN				LAD 2			
2	LAD 1							
3	LAD Ø							

Definition of these bytes is as follows:

Byte Ø - Sense Byte - This byte describes the details or nature of an error status. The bits within the Sense Byte are defined as:



Bit 7 - Valid Block Address - This bit, when set, indicates that the Logical Sector Address, the LAD in bytes 1 through 3,contains the valid logical address of the block at which the error occurred.

Bit 5 and Bit 4 - Error Type - These two bits describe the general type of Error as follows:

ØØ = Drive related error
Ø1 = Controller related error
1Ø = Command related error
11 = Miscellaneous error

Bits 3 through Ø - Error Code - These bits define the error under each of the four types of errors defined by bits 4 and 5. The Error Codes are given in Table 3-2.

3.2.4 OpCode Ø3 (Request Sense) (continued)

Byte 1 - LUN and LAD 2 - LUN (bits 7,6, and 5) indicates the logical unit number of the drive where the error occurred. LAD 2 (bits 4,3,2,1, and Ø) are the five most significant bits of the Logical Sector Address.

Byte 2 - LAD 1 - The eight center bits of the Logical Sector Address.

Byte 3 - LAD Ø - The eight least significant bits of the Logical Sector Address.

NOTE: Logical Address (LAD Ø,1 and 2) is valid only if the Block Address Valid bit (Byte Ø, bit 7) is set in the Sense byte.

TABLE 3-2

Sense Byte Error Codes

Type Ø (Drive) Error Codes

Ø	No Error Status
1	No Index Signal
2	No Seek Complete
3	Write Fault
4	Drive Not Ready
5	Drive Not Selected
6	No Track ØØ
7	Multiple Winchester Drives Selected
9	Media Change. This status indicates that the removeable media was changed since the last command was issued to the requested unit. This status will be reported the first time a command which reads or writes on the media is issued after the media change. The requested command will not be performed. This condition is cleared for the NEXT I/O.
D	Seek in Progress

Type 1 (Controller) Error Codes

Ø	ID Read Error (ECC) error in the ID field
1	Uncorrectable Data Error during a Read
2	ID Address Mark not found
3	Data Address not found
4	Record not found (Found correct cylinder and head but not sector)
5	Seek Error (R/W head positioned on a wrong cylinder and/or selected on wrong head
6	Unused
7	Write Protected
8	Correctable Data Field Error
9	Bad Block Found
A	Format Error (the Controller detected during a Check Track command that the format on the drive was not as expected)
C	Unable to Read an Alternate Track Address
E	Attempted to directly access an alternate track.
F	Sequence Time Out during Disk or Host Transfer

Type 2 (Command) Error Codes

Ø	Invalid Command received from the Host
1	Illegal Disk Address (address beyond the maximum address)
2	Illegal Function for type of drive specified
3	Volume Overflow - Maximum sector address was passed during a multiple sector read or write

Type 3 (Miscellaneous) Error Code

Ø	RAM Error

3.2.5 OpCode Ø4 (Format Drive)

This command formats all the tracks on the specified drive with the selected track format. The sectors will be placed on the tracks according to the interleave code specified in the command block and the data fields will be filled with "E5 Hex" (111ØØ1Ø1).

NOTE: The Interleave Code (byte 4) is ignored in the KODAK/DRIVETEK floppy because the media is preformatted.

The required fields for this command are: OPCODE, LUN and INTERLEAVE CODE.

	MSB						LSB
BYTE #	7	6	5	4	3	2	1	Ø
Ø	Ø	Ø	Ø	Ø	Ø	1	Ø	Ø
1	LUN					Ø		
2	Ø							
3	Ø							
4	INTERLEAVE CODE							
5	Ø							

See the flowchart in Figure 3-6 for additional information on this command, see Appendix B for additional information on interleave, and Appendix C for additional information on disk format.

Class Code 0
OpCode 04

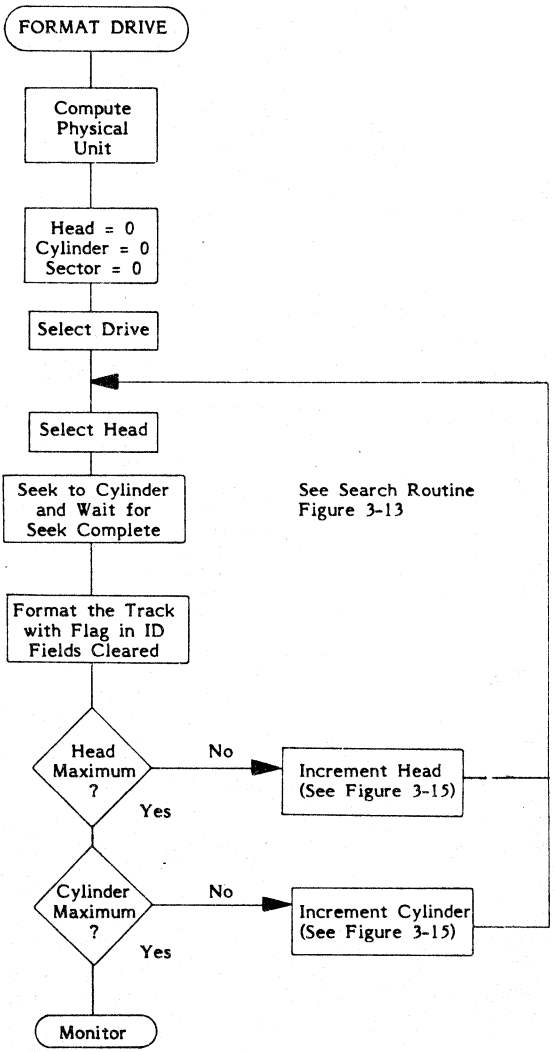


Figure 3-6 Format Drive Command

3.2.6 OpCode Ø5 (Check Track Format) (not valid for floppy)

This command checks the ID Fields and the interleave of the sectors on the specified tracks for correctness. The specified Logical Address (LAD) may fall anywhere in the track and the entire track will be checked. This command does not read or check the data fields.

The required fields for this command are: OPCODE, LUN LAD 2, LAD 1, LAD Ø, and INTERLEAVE CODE.

	MSB						LSB
BYTE #	7	6	5	4	3	2	1	Ø
Ø	Ø	Ø	Ø	Ø	Ø	1	Ø	1
1	LUN				LAD 2			
2	LAD 1							
3	LAD Ø							
4	INTERLEAVE CODE							
5	Ø							

Class Code 0
OpCode 05

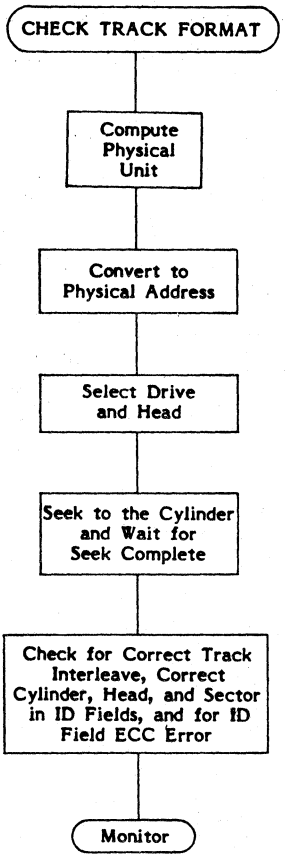


Figure 3-7 Check Track Format Command

3.2.7 OpCode Ø6 (Format Track)

This command formats all sectors of the specified tracks with no flags set in the ID fields. The sectors will be placed on the track according to the Interleave Code specified in Byte 4 and data fields will be filled with E5 Hex (11100101). The specified Logical Address (LAD) may fall anywhere in a track and the entire track will be formatted.

NOTE: The Interleave Code (byte 4) is ignored in the KODAK/DRIVETEK floppy.

The required fields for this command are: OPCODE, LUN, LAD and INTERLEAVE.

	MSB							LSB
BYTE #	7	6	5	4	3	2	1	Ø
Ø	Ø	Ø	Ø	Ø	Ø	1	1	1
1	LUN				LAD 2			
2	LAD 1							
3	LAD Ø							
4	INTERLEAVE CODE							
5	Ø							

See the flowchart in Figure 3-8 for additional information on this command, Appendix B for Interleave information and Appendix C for Format information.

Class Code 0
OpCode 06

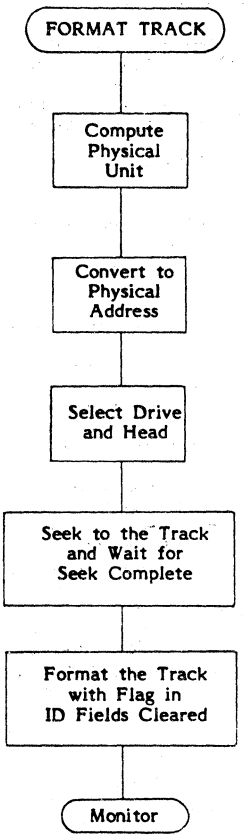


Figure 3-8 Format Track Command

3.2.8 OpCode Ø7 (Format Bad Track) (not valid for floppy)

This command will format the specified track with the bad block flag set in all ID fields on the track. The sectors will be placed on the track according to the Interleave Code specified in Byte 4 and data fields will be filled with E5 Hex (111ØØ1Ø1) binary). The specified Logical Address (LAD) may fall anywhere in a track and the entire track will be formatted.

The required fields for this command are: OPCODE, LUN, LAD and INTERLEAVE.

	MSB							LSB
BYTE #	7	6	5	4	3	2	1	Ø
Ø	Ø	Ø	Ø	Ø	Ø	1	1	1
1	LUN				LAD 2			
2	LAD 1							
3	LAD Ø							
4	INTERLEAVE CODE							
5	Ø							

See the flowchart in Figure 3-9 for additional information on this command, Appendix B for Interleave information and Appendix C for Format information.

Class Code 0
OpCode 07

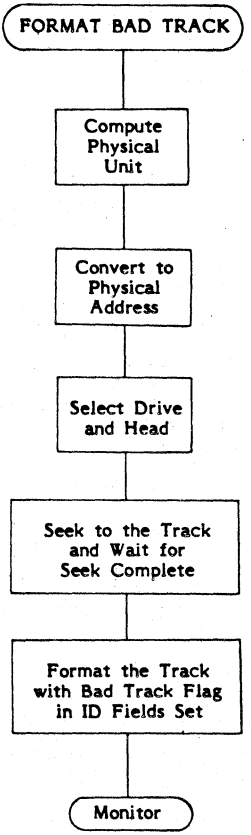


Figure 3-9 Format Bad Track Command

3.2.9 OpCode Ø8 (Read Block)

This command reads the specified number of blocks (Sectors starting from the initial block address given in the LAD fields and transfers them to the Host.

The required fields for this command are: OPCODE, LUN, LAD 2, LAD 1, LAD Ø, # OF BLOCKS, and CONTROL.

	MSB							LSB
BYTE #	7	6	5	4	3	2	1	Ø
Ø	Ø	Ø	Ø	Ø	1	Ø	Ø	Ø
1	LUN				LAD 2			
2	LAD 1							
3	LAD Ø							
4	NUMBER OF BLOCKS							
5	CONTROL							

See the flowchart in Figure 3-1Ø for additional information on this command.

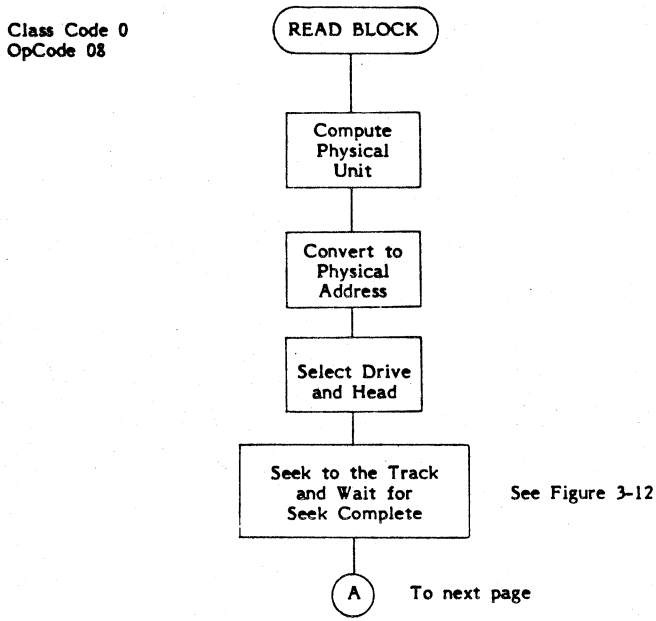


Figure 3-10 Read Block Command (Sheet 1 of 2)

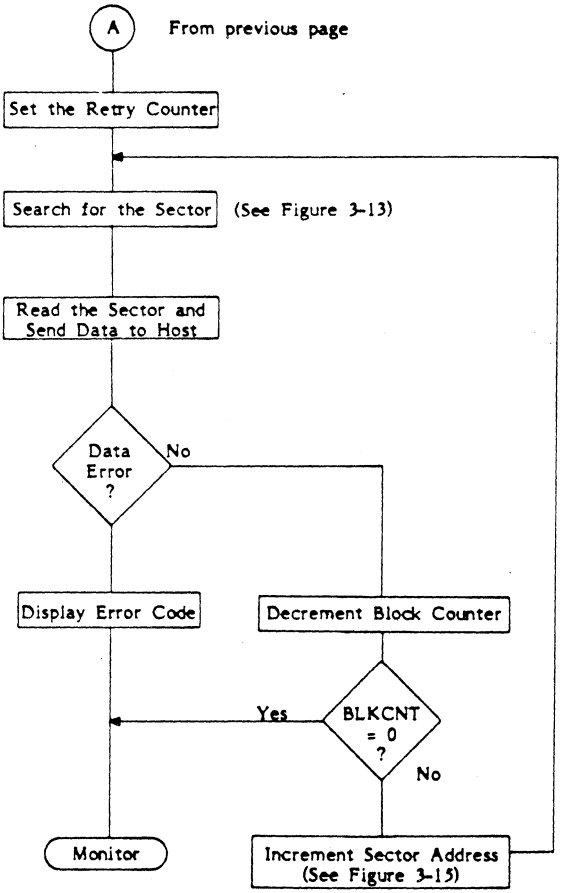


Figure 3-10 Read Block Command (Sheet 2 of 2)

3.2.1Ø Opcode ØA (Write Block)

This command gets the data from the Host and writes the specified number of blocks (Sectors) starting from the initial block address given in the LAD fields.

The required fields for this command are: OPCODE, LUN, LAD 2, LAD 1, LAD Ø, # OF BLOCKS, and CONTROL.

	MSB							LSB
BYTE #	7	6	5	4	3	2	1	Ø
Ø	Ø	Ø	Ø	Ø	1	Ø	1	Ø
1	LUN			LAD 2				
2	LAD 1							
3	LAD Ø							
4	NUMBER OF BLOCKS							
5	CONTROL							

See the flowchart in Figure 3-11 for additional information on this command.

Class Code 0
OpCode 0A

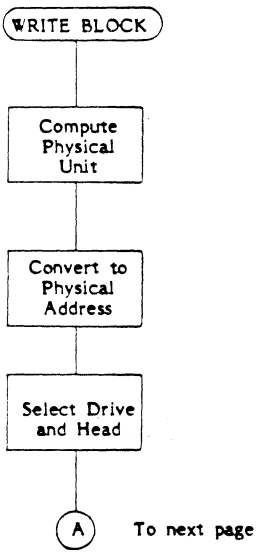


Figure 3-11 Write Block Command (Sheet 1 of 2)

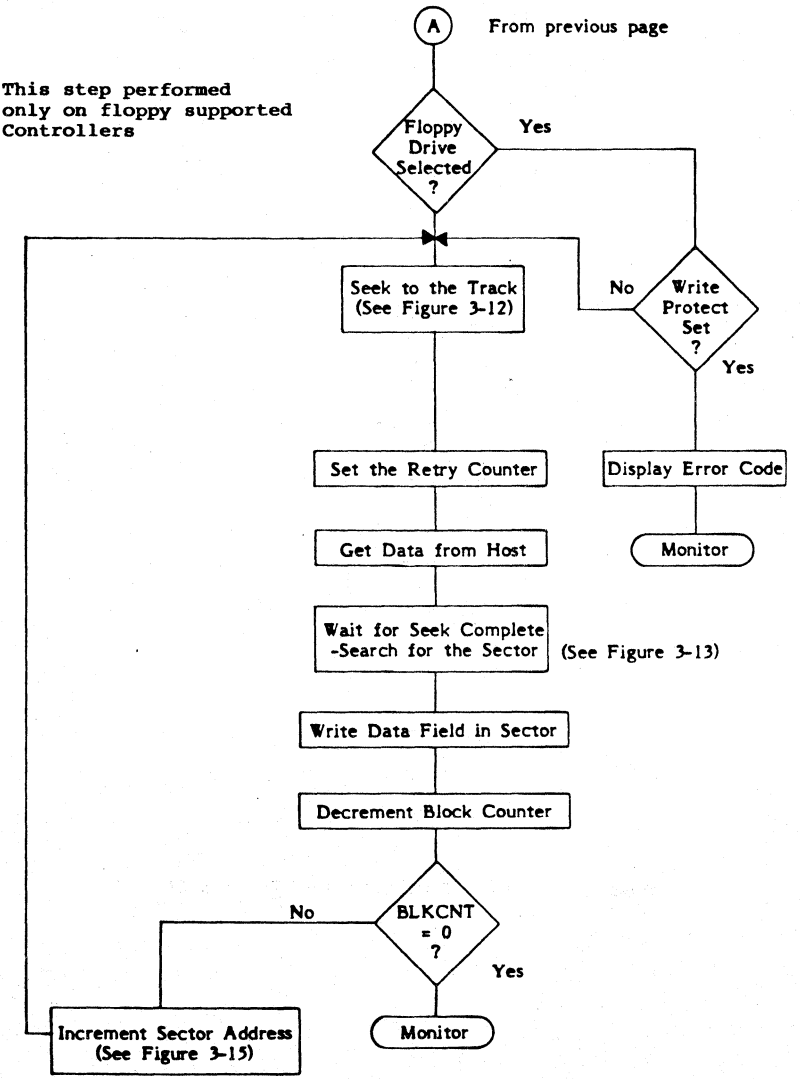


Figure 3-11 Write Block Command (Sheet 2 of 2)

3.2.11 OpCode ØB (Seek)

This command initiates a seek to the cylinder where the block specified in the LAD field is located. For Winchester drives capable of doing Overlap Seeks (depending on how the drive parameter is set up) this command could immediately return Completion Status before the Seek Complete (from the drive) is found. Normally this command returns the Completion Status only after the seek in completed.

The required fields for this command are: OPCODE, LUN, LAD 2, LAD 1, and LAD Ø.

	MSB						LSB
BYTE #	7	6	5	4	3	2	1	Ø
Ø	Ø	Ø	Ø	Ø	1	Ø	1	1
1	LUN			LAD 2				
2	LAD 1							
3	LAD Ø							
4	Ø							
5	Ø							

See flowchart in Figure 3-12 for additional information on this command.

Class Code 0
OpCode 0B

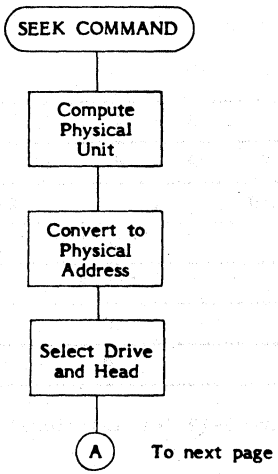


Figure 3-12 Seek Command (Sheet 1 of 2)

This step performed only with floppy supported Controllers

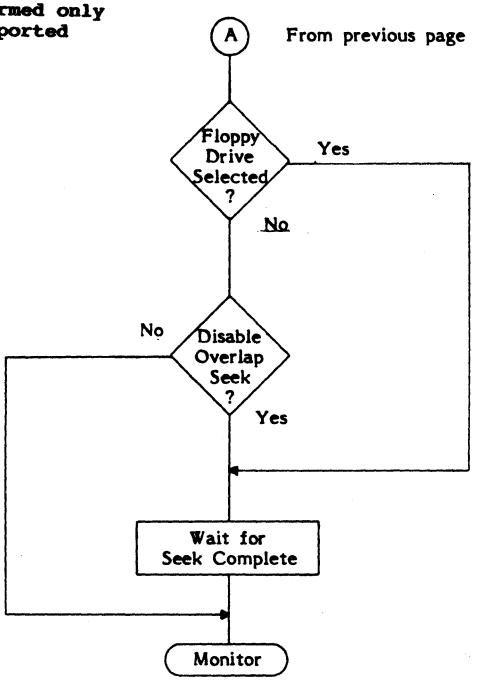


Figure 3-12 Seek Command (Sheet 2 of 2)

3.2.12 OpCode ØD (Select Interleave Factor) (KODAK 3.3 only)

In order to allow the Controller to work with variable Host system speeds the Controller will modify the strict logical to physical address correlation by selecting an interleave factor.(This applies to read, and write commands). The interleave is in byte 4 of the CDB. The interleave factor minus one (1) specifies the number of physical sectors between two consecutive logical sectors, Thus an interleave factor of 2 will mean that logical sector Ø is Ø , but logical sector 1 is physical sector 2 (skipping sector 1). The default interleave factor is one (1) upon power up or reset. Commands with interleave code Ø will be interpreted as an interleave code of one (1).

Byte #	7	6	5	4	3	2	1	Ø
Ø	Ø	Ø	Ø	Ø	1	1	Ø	1
1	LUN			Set to Ø				
2	Set to Ø							
3	Set to Ø							
4	INTERLEAVE CODE							
5	Set to Ø							

The required fields for this command are: OPCODE, LUN and INTERLEAVE CODE.

Example of sector ordering for interleave factor of 2 with 17 sector/track:

Phy sec:	Ø	1	2	3	4	5	6	7	8	9	1Ø	11	12	13	14	15	16
Log sec:	Ø	9	1	1Ø	2	11	3	12	4	13	5	14	6	15	7	16	8

3.2.13 OpCode ØE (Assign Alternate Track) (not valid for floppy)

This command formats the track specified in the LAD with the alternate Bad Track Flag set in the ID Fields and with the track address of the Alternate Track written in the data fields. This command also formats the Alternate Track with the alternate Track Indentifier Flag set in its ID fields and data pattern E5 Hex (111ØØ1Ø1 binary) written in the data fields.

Future Read or Write commands, to the track with the Alternate Bad Track Flag set, will cause the drive to seek to the Alternate Track address, transparent to the Host software, and the Read or Write operation would be performed at the Alternate Track.

NOTE: Alternate tracks can be assigned one level only, i.e. an Alternate Track cannot be assigned an alternate track.

The required fields for this command are: OPCODE, LUN, LAD 2, LAD 1, LAD Ø, INTERLEAVE, and CONTROL.

See the Appendices for additional information on Interleave and Formats.

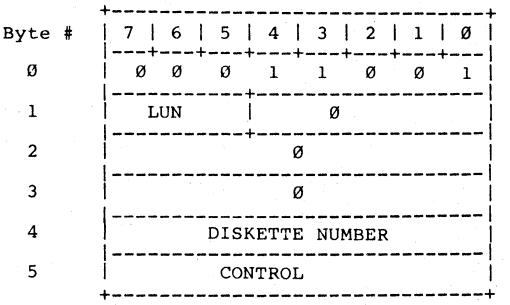
	MSB							**LSB**
BYTE #	7	6	5	4	3	2	1	Ø
Ø	Ø	Ø	Ø	Ø	1	1	1	Ø
1	LUN				LAD 2			
2	LAD 1							
3	LAD Ø							
4	NUMBER OF BLOCKS							
5	CONTROL							

After the Controller receives this command, it will collect the alternate Track Address as data (C/D deasserted) from the Host in the following format:

	MSB							LSB
BYTE #	7	6	5	4	3	2	1	Ø
Ø	Ø	Ø	Ø	LAD 2				
1	LAD 1							
2	LAD Ø							

3.2.14 **Opcode 19 (Media Select) (535B Amyln only)**

This command allows the Host to select which diskette in an Amlyn cartridge is to be loaded.



Required fields are: Opcode, LUN, Byte 4 and CONTROL. Byte 4 may be in the limits Ø to 4.

3.3 **Routines**

This section contains flowcharts of the Search, Random Read, and Increment Sector or Head routines. These routines are called out in the flowcharts explaining the commands (OpCodes)

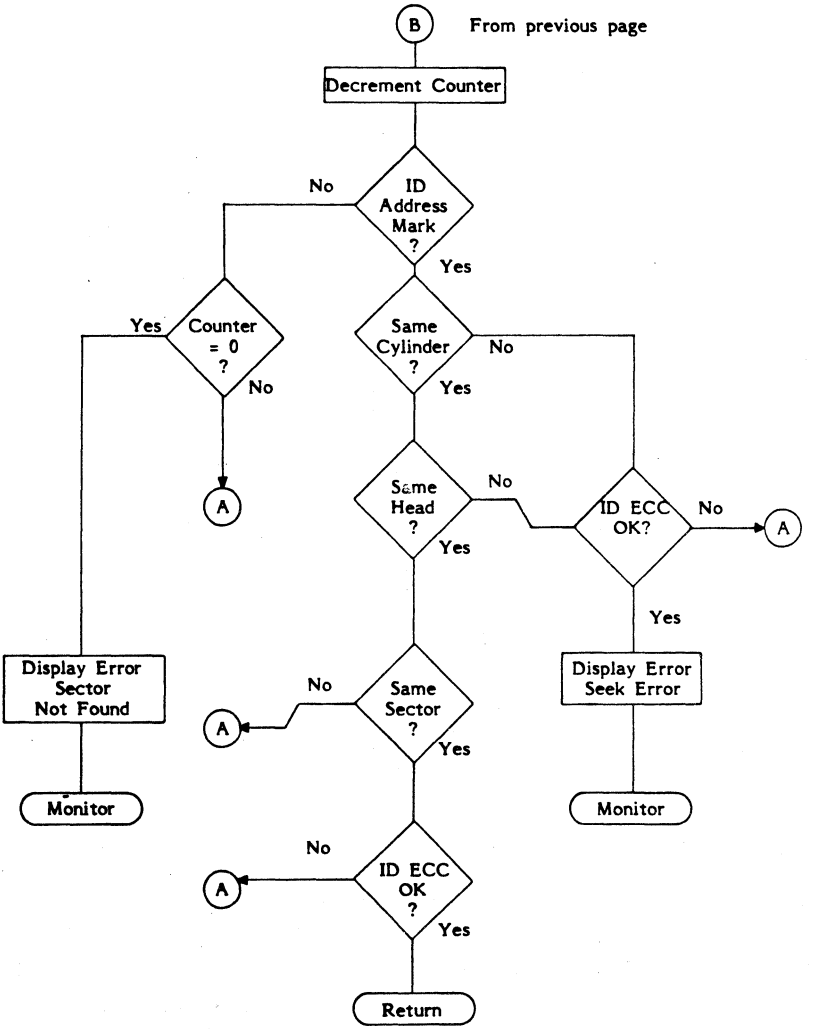


Figure 3-13 Search Routine (Sheet 2 of 2)

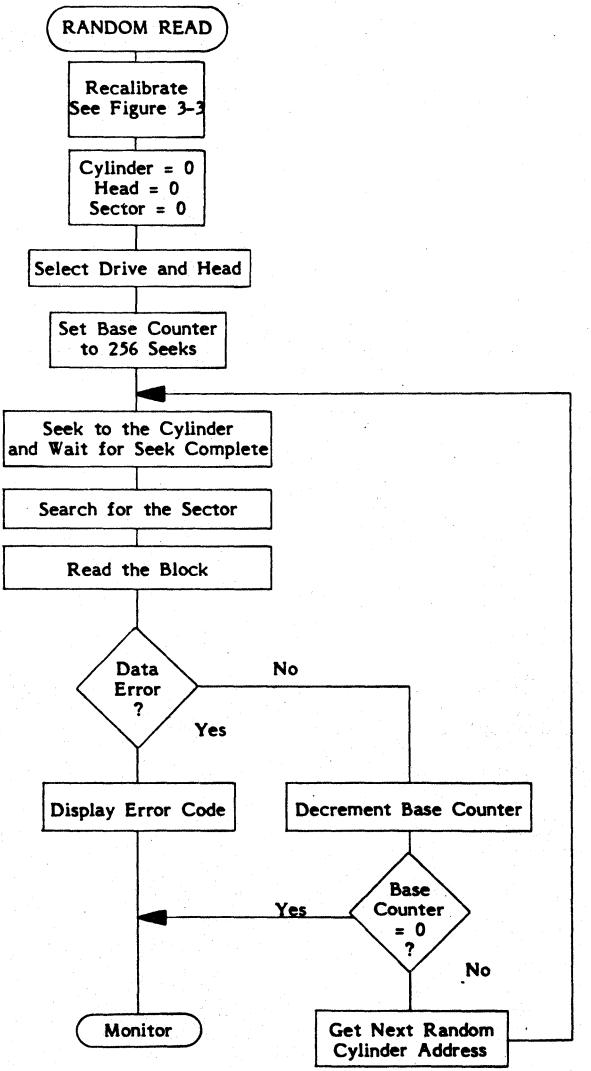


Figure 3-14 Random Read Routine

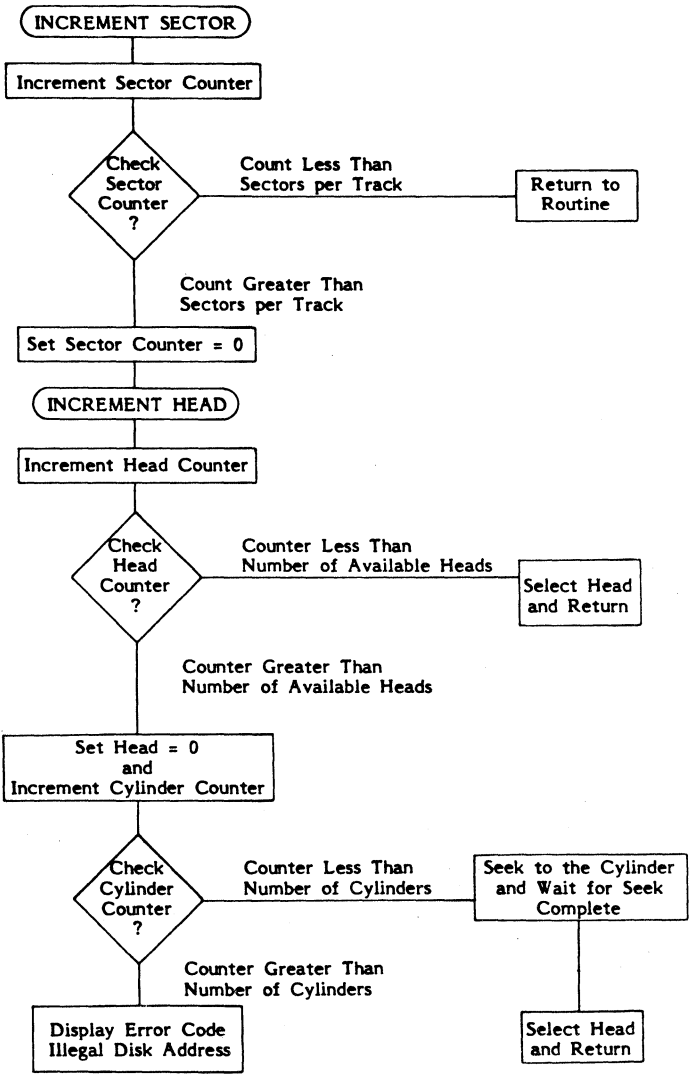


Figure 3-15 Increment Sector, Head, or Cylinder

3.4 Class Code 1 Commands

Only one OpCode is implemented with a Class Code 1 CDB (Command Descriptor Block). This is the Copy OpCode (ØØ Hex). The Copy OpCode will cause the number of sectors specified by Byte 4 to be copied from the Source LUN (Byte 1) to the Destination LUN (Byte 5). The starting address on the Source Drive is specified by Bytes 1, 2, and 3. The starting address on the Destination Drive is specified by Logical Address Bytes 5, 6, and 7. Byte 8 is reserved as a spare. Byte 9 is the Control Byte.

This command reads a sector (data block) from the specified starting address of the Source Drive and writes it at the specified starting address of the Destination Drive. With each sector transferred, the Source and the Destination addresses are incremented, and the Sector Count (Byte 4) is decremented. The operation continues until the Sector Count (Byte 4) is zero.

The format and the significance of the ten byte CDB used with this OpCode is shown below. See flowchart in Figure 3-16.

	MSB							**LSB**
BYTE #	7	6	5	4	3	2	1	Ø
Ø	Ø	Ø	1	Ø	Ø	Ø	Ø	Ø
1	Source - LUN			Source - LAD 2				
2	Source - LAD 1							
3	Source - LAD Ø							
4	Number of Sectors to be Copied from Source							
5	Dest. - LUN			Dest. - LAD 2				
6	Destination - LAD 1							
7	Destination - LAD Ø							
8	Ø							
9	Control Byte							

CAUTION: The results of the copy command are unpredictable if there is a change in sector size (for example, track Ø on a floppy with a different sector size than all other tracks on the diskette).

3.4.1 Class Code 5 Commands (510B only)

Byte #	7	6	5	4	3	2	1	Ø
Ø	1	Ø	1	OPCODE				
1	LUN/s			LAD 2/s*				
2	LAD 1/s*							
3	LAD Ø/s*							
4	LUN/d			LAD 2/d*				
5	LAD 1/d*							
6	LAD Ø/d*							
7	# OF BLOCKS 2							
8	# OF BLOCKS 1							
9	# OF BLOCKS Ø							
1Ø	Ø							
11	CONTROL							

"s" = the source device
"d" = the destination device.

*Refer to Appendix A for Logical Address Computation

NOTE: Lun/s, Lun/d and logical addresses are only applicable to the disk drives.

Command Description (GROUP 5) (510B only)

OPCODE (Hex)	DESCRIPTION
ØØ	COPY. This command transfers the data blocks from the specified source device location to the specified destination device location. The number of data blocks to copy is specified in the number of blocks field (byte 7 - byte 9 is LSB). If the field is zero, 16,777,216 blocks will be copied.

Class Code 1
OpCode 00

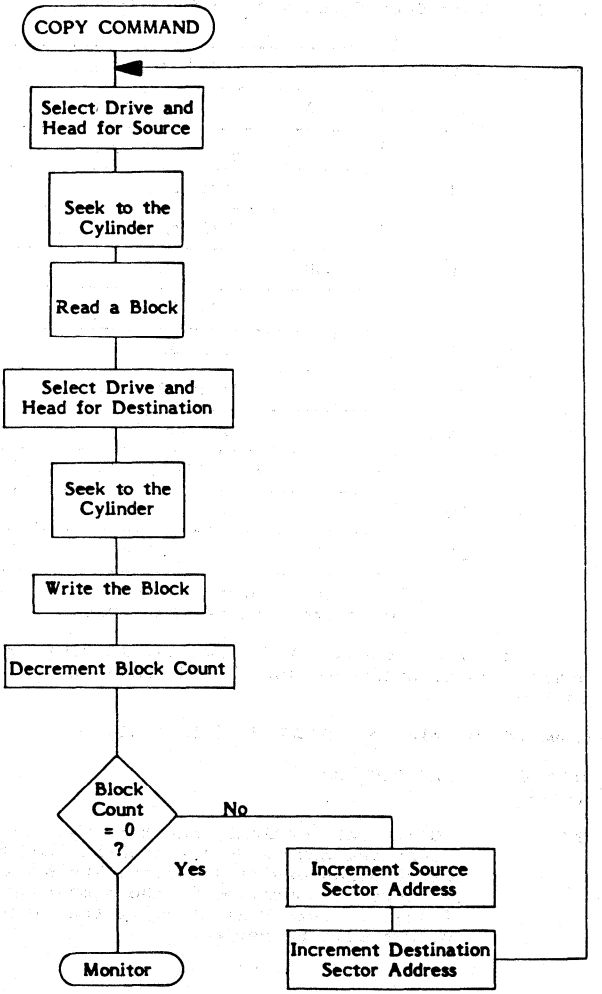


Figure 3-16 Copy Command

3.5 Class Code 6 Commands

There are three OpCodes in this Class Code:

OpCode ØØ - Used only with the 520B and 535B, to define the track format of the Floppy Disk Drive, or (depending on the value in byte 2 of the CDB) to enable/disable the double step function.

OpCode Ø1 - Used with the 535B to set up drive parameters for several popular 8 inch floppy drives without having to specify all of the drive parameters. The drive type is located in Byte 4 of the command block and the particular LUN must have been preassigned as a floppy for this command to function.

OpCode Ø2 - Used with the 500B Series Controller to set the parameters of the drive, Opcode Ø2 is explained in Paragraph 3.5.?.

3.5.1 OpCode ØØ (Define Track Format of Floppy Drive or Enable/ Disable Double Step Function) (520B, 535B)

The required fields for this command are: OPCODE, LUN, BYTE 2, BYTE 4, and CONTROL.

When the value of byte 2 of the CDB is set to "Ø" this OpCode will define the Track Format used with the selected Floppy Disk Drive. When the value of byte 2 of the CDB is set to "1" this OpCode will Enable/Disable the double step function.

	MSB							LSB
BYTE #	7	6	5	4	3	2	1	Ø
Ø	1	1	Ø	Ø	Ø	Ø	Ø	Ø
1	LUN				Set to Ø			
2	(Ø Track Format)				(1 Double Step)			
3	Set to Ø							
4	See Note 1							
5	See Note 2							

3.5.1 OpCode ØØ (continued)

Note 1: When Byte 2 is set to Ø (Define Track Format)
Set all bits of Byte 4 to zero.
When Byte 2 is set to 1 (Define Double Step Function)
Set bit Ø of Byte 4 to zero to disable double step function.
Set bit Ø of Byte 4 to 1 to enable doule step fuction.

NOTE 2: When Byte 2 is set to Ø (Define Track Format)
Set Byte 5 to one of the Hex codes given in Table 3-3 to set the parameters of the Floppy drive.
When Byte 2 is set to 1 (Define Double Step Function)
Set all bits of Byte 5 to zero.

3.5.1.1 Define Track Format - OpCode ØØ and Byte 2 Set to Ø

Byte 5 of this command defines the Track Format of the Selected Floppy disk drive connected to the Controller. The Hex code given in Table 3-3, that corresponds to the Track Format of the selected Floppy drive is placed in Byte 5 of the CDB.

TABLE 3-3

Floppy Drive Track Format (Byte 5 Class Code 6)

Track Format Code (Hex)	Track Format Set for Floppy Drive
ØØ	Single density, Single-sided, FM recorded with 128 bytes Sector/16 Sector per Track (26 Sectors per Track on 535B).
Ø1	Single density, Double-sided, FM recorded with 128 bytes Sector/16 Sectors per Track (26 Sectors per Track on 535B).
Ø6	Double density, Single-sided, Cylinder Ø - FM recorded with 128 bytes Sector/16 Sectors per Track (26 Sectors per Track on 535B); all other cylinders - MFM recording with 256 bytes Sector/16 Sectors per Track (26 Sectors per Track on 535B).
Ø7	Double density, Double-sided, Head Ø, Cylinder Ø - FM recorded with 128 bytes Sector/16 Sectors per Track (26 Sectors per Track on 535B); all other tracks MFM recording with 256 bytes Sectors/16 Sectors per track (26 Sectors per Track on 535B).
86	Double density, Single-sided, MFM recording with 256 bytes Sector/16 Sectors per Track (26 Sectors per Track on 535B).
87	Double density, Double-sided, MFM recording with 256 bytes Sector/16 Sectors per Track (26 Sectors per Track on 535B).

Table 3-3 Floppy Drive Track Format (continued)

8A	Double density, Single-sided, MFM recording with 512 bytes Sector/8 Sectors per Track (15 Sectors per Track on 535B).
8B	Double density, Double-sided, MFM recording with 512 bytes Sectors/8 Sectors per Track (15 Sectors per Track on 535B).
8E	Double density, Single-sided, MFM recording with 1,Ø24 bytes Sector/5 Sectors per Track (8 Sectors per Track on 535B).
8F	Double density, Double-sided, MFM recording with 1,Ø24 bytes Sector/5 Sectors per Track (8 Sectors per Track on 535B).

NOTE 1: For the 52ØB, the default mode, which will occur after each Reset or Power-on, will be the same as specified with 8A Hex.

NOTE 2: For the 535B, if track format information for floppy is not specified after each reset or power-on, the default code will be the same as specified with ØØ Hex.

3.5.1.2 Define Double Step Function - OpCode ØØ Byte 2 Set to 1

Bit Ø of Byte 4 is set to enable the Double Step Function. This function allows a 96 TPI Floppy disk drive to read/write a diskette at 48 TPI.

Bit Ø of Byte 4 is set to Ø to disable the Double Step Function.

3.5.1.3 Define KODAK 3.3 Floppy Media and Track Format

The Class 6, OpCode ØØ command is subdivided into three commands. The sub-command opcode is specified in byte 2 of the CDB.

Sub-opcode	Description
Ø	Reserved
1	Reserved
2	Define KODAK 3.3 Minifloppy Disk Track Format and floppy media.

OpCode ØØ, Sub-Opcode Ø2

This command is used to define the number of bytes per sector and the number of sectors per track for KODAK 3.3 drive. It is also used to define the tracks per inch, number of bytes per sector, the number of sectors per track, FM or MFM recording and number of sides when KODAK Drive 3.3 is used to read the conventional 48tpi or 96tpi diskettes.

Byte #	7	6	5	4	3	2	1	Ø
Ø	1	1	Ø	Ø	Ø	Ø	Ø	Ø
1	LUN				Ø			
2	Ø	Ø	Ø	Ø	Ø	Ø	1	Ø
3	tpi		S	D	Ø	Ø	SIZE	
4	Number of sectors per track							
5	Ø							

Byte 3 Bit 7 -- 6 TPI

Ø Ø - 192tpi
Ø 1 - 96tpi
1 Ø - 48tpi

Bit 5 Number of sides

Ø - single sided
1 - double sided

Bit 4 Recording density

Ø - FM
1 - MFM

Bit 1 - Ø Sector Size

Ø Ø 128 bytes per sector
Ø 1 256 bytes per sector
1 Ø 512 bytes per sector
1 1 1Ø24 bytes per sector

Sub-Opcode Ø2 (continued)

Byte 4 Number of sectors per track

E.G. for a 256 bytes/sector, 3Ø sectors/track floppy
set byte 3 to Ø1 (Hex)
and set byte 4 to 1E (Hex).

NOTE 1: For 192tpi media only double-sided, double density is allowed. so Bit 5 - 4 of Byte 3 will be ignored.

NOTE 2: If the floppy is not specified after each reset or power on, the default code will be as follows:

192tpi media
512 Bytes/Sector
17 Sectors/Track

The required fields for this command are: OPCODE, LUN SUB-OPCODE (Byte 2) TPI CODE, SIDE, DENSITY, NUMBER OF BYTES PER SECTOR and NUMBER OF SECTORS PER TRACK.

3.5.2 OpCode Ø1 (Assign Drive Type) (535B Floppy only)

This command allows the Host to set up drive parameters for several popular 8 inch floppy drives without having to specify all of the drive parameters. The drive type is located in Byte 4 of the command block and the particular LUN must have been preassigned as a floppy for this command to function.

The value placed in Byte 4 determines what type of 8 inch floppy drive is being used.

Byte 4	Drive Type		
2	SA8ØØ or Tandon	TM848-1	8ms step.
3	SA85Ø or Tandon	TM848-2	3ms step.

NOTE 1: When using two 8 inch floppies LUN 2 and LUN 3 must represent the floppy drives.

NOTE 2: When using one AMLYN drive and one 8 inch floppy drive, the 8 inch floppy drive must be LUN 3.

NOTE 3: Upon power up or reset the Controller will default to the SA8ØØ/8Ø1 drive

Byte #	7	6	5	4	3	2	1	Ø
Ø	1	1	Ø	Ø	Ø	Ø	Ø	1
1	LUN				Set to Ø			
2	Set to Ø							
3	Set to Ø							
4	Drive Type Code							
5	Set to Ø							

The required fields for this command are: OPCODE, LUN and DRIVE TYPE FORMAT.

3.5.3 OpCode Ø2 (Set Drive Parameters) (not valid for KODAK 3.3 or floppies on 535B)

The Host must set the parameters only when using a drive with parameters that differ from the ST5Ø6. The DTC-5ØØB Series will set the ST5Ø6 drive parameters (the default parameters) in the Controller after power is applied and after each reset.

This command permits different manufacturer's drives to be used with each LUN. The required fields for this command are OPCODE and LUN.

	MSB						LSB
BYTE #	7	6	5	4	3	2	1	Ø
Ø	1	1	Ø	Ø	Ø	Ø	1	Ø
1	LUN			Set to Ø				
2	Set to Ø							
3	Set to Ø							
4	Set to Ø							
5	Set to Ø							

Ten (1Ø) bytes of drive parameters will be collected from the Host as Data (C/D deasserted) after this command. The format of this data will be different for a Winchester than for a Floppy disk drive.

With the DTC-52ØB and 535BK, switches 7 and 8 on the Controller defines LUN Ø and LUN 1 as either a Winchester or Floppy drive.

With the DTC 535B LUN Ø and LUN 1 are always a hard disk.

With the DTC-51ØB only the Winchester Drive parameters are used.

3.5.3.1 Winchester Drive Parameters

The parameters for a Winchester drive are passed as data to the Controller using the following format:

	MSB							LSB
BYTE #	: 7 :	6 :	5 :	4 :	3 :	2 :	1 :	Ø :
Ø	:Step Pulse Width (Default is 13.6 usec)							(11):
1	:Step Period (Default is 3 milliseconds)							(6Ø):
2	:Step Mode (Default is Buffered)							(Ø):
3	:Maximum Head Address (Default is 4 heads)							(3):
4	:High Cylinder Address byte(Default set to Ø)							(Ø):
5	:Low Cylinder Address byte(Default is 153 cylinders)							(152):
6	:Reduce Write Current (Default is above Cylinder 128)							(127):
7	:Drive Type/ Seek Complete Option							(Ø):
8	:Set to Ø							(Ø):
9	:Set to Ø							(Ø):

NOTE: Default condition is given in parenthesis immediately after the parameter definition. Default value is shown (in decimal) in the parenthesis on the right.

Definition of format for Winchester Drive parameters are:

Byte Ø - Step Pulse Width - The time Step signal is asserted. Range is 6.8 to 217.6 microseconds.

Byte Ø Value	Step Pulse Width
1 to 6	6.8 microseconds
7 to 13	13.6 microseconds
14 to 2Ø	2Ø.4 microseconds
21 to 27	27.2 microseconds
28 to 34	34.Ø microseconds
.	
.	
242 to 248	21Ø.8 microseconds
249 to 255	217.6 microseconds

3.5.3.1 **Winchester Drive Parameters** (continued)

Byte 1 - Step Period - The time Step pulse is deasserted between two consecutive Step Pulses, given in 50 microsecond increments. Range is 50 microseconds to 12.8 milliseconds.

Hex Value of Byte 1	Step Period
01	50 microseconds
02	100 microseconds
03	150 microseconds
.	
.	
FF	12.8 milliseconds

Byte 2 - Step Mode - Defines 1 of 2 stepping modes for the drive:

Mode 0 - Normal or Buffered Step mode, this mode generates step pulses using values specified in Bytes 0 and 1.

Mode 4 - 13 us step period.

Byte 3 - Maximum Head Address - Defines the maximum head address on the drive. Range is 0 to 7 (i.e. 1 to 8 heads). Optional firmware Range is 0 to 15 (i.e., 1 to 16 heads).

Byte 4 - High Cylinder Address Byte - Defines the value of the upper bits of the cylinder address of the drive. Range is 256 to 1,023.

Byte 5 - Low Cylinder Address Byte - Defines the value of the lower 8 bits of the cylinder address of the drive. Range is 0 to 255.

NOTE: Bytes 4 and 5 define the maximum cylinder address range as 00 to 1,023 (i.e. up to 1,024 cylinders).

3.5.3.1 **Winchester Drive Parameters** (continued)

Byte 6 - Reduce Write Current - Specifies the cylinder address where the current supplied to the Read/Write heads is reduced. Range is Ø to 255. If this value is set to "Ø", the write current is never asserted. When the default value of 128 is set in this byte, the write current applied (during all disk write operations) at cylinder address 128 and greater is reduced. When using optional firmware and when selecting more than eight (8) heads, this line is used as a head select line.

Byte 7 - Drive Type Identifier - This byte must be set as follows:

Bit 7 - Set to Ø to indicate parameters are for hard disk.

Bit 6 - Set to Ø indicates wait for a Seek Complete signal from the drive after the last Step pulse has been sent. Set to 1 indicates do not wait for Seek Complete signal from the drive after the last step pulse has been sent.

Bits 5 through Ø - Set to Ø.

Bit 6 - Used to utilize the overlap seek function if it is built into the drive.

NOTE: The Seek Incomplete timeout is set to approximately 7ØØ milliseconds and any seek that does not complete within 7ØØ milliseconds will be flagged as an error.

Byte 8 - Set to Ø (Reserved)

Byte 9 - Set to Ø (Reserved)

3.5.3.2 **Floppy Drive Parameters** (520B only)

The parameters for a Floppy drive are passed as data to the Controller using the following format:

	MSB						**LSB**
BYTE #	7	6	5	4	3	2	1 Ø
Ø	Step Pulse Width (Default is 17 microseconds)						(2)
1	Step Interval (Default is 7 milliseconds)						(7)
2	Maximum Cylinder Address (Default is 8Ø)						(79)
3	Head Setting Time (Default is 22 milliseconds)						(22)
4	Time for Valid Data after Head Select(Default 2Ø5us)						(2Ø5)
5	Time for Valid Data after Drive Select(Default Ø msec)						(Ø)
6	Delay After Write Gate Deasserted (Default 1.1 msec)						(11)
7	Mini Floppy Parameters Indicator						(128)
8	Set to Ø						(Ø)
9	Set to Ø						(Ø)

NOTE: Default condition is given in parenthesis immediately after the parameter definition. Dfault value is shown (in decimal) in the parenthesis on the right.

3.5.3.2 Floppy Drive Parameters (continued)

Definition of format for Floppy Drive parameters are:

Byte Ø - Step Pulse Width - The time signal is asserted. Range is 17 to 255 microseconds.

Byte Ø Value	Step Pulse Width
1 to 17	17.Ø microseconds
18 to 24	25.5 microseconds
26 to 34	34.Ø micorseconds
35 to 42	42.Ø microseconds
43 to 51	51.Ø microseconds
52 to 59	59.5 micorseconds
6Ø to 68	68.Ø microseconds
.	.
.	.
237 to 246	246.5 microseconds
247 to 255	255.Ø microseconds

Byte 1 - Step Interval - The time Step Pulse is deasserted between two consecutive Step Pulses, in 1 millisecond increments. Range is 1 millisecond to 256 milliseconds.

Hex Value of Byte 1	Step Period
Ø1	1 millisecond
Ø2	2 milliseconds
Ø3	3 milliseconds
.	.
.	.
FF	256 milliseconds

Byte 2 - Specifies the number of tracks in the drive.

Byte 3 - Head Settling Time - Defines the period of time from the last Step pulse to the time valid Read/Write data transfers can be accomplished. Range is 1 to 256 milliseconds in 1 millisecond increments.

Byte 4 - Time Before Valid Data After Head Select - Defines the period of time from a change in the Selected Head to the time valid Read/Write data tranfers can be accomplished. Range is 1 to 256 usec.

3.5.3.2 Floppy Drive Parameters (continued)

Byte 5 - Time Before Valid Data After Drive Select - Defines the period of time from a change in Select Drive to the time valid Read/Write data transfers can be accomplished. Range is 1 to 256 milliseconds. If this value is set to "Ø" this delay will not be applied.

Byte 6 - Delay After Write Gate is Deasserted - Defines the period of time from the deassert of Write Gate to the Time Valid Read data, Head Select, Drive Select, or Next Step Sequence is accepted. Range is Ø to 25.5 milliseconds in 1ØØ microsecond increments. If this value is set to "Ø", this delay will not be applied.

Byte 7 - Drive Type Identifier - This byte must be set as follows:

Bit 7 - Set to 1 to indicate parameters are for mini-floppy.
Bit 6 through Ø - Set to Ø.

Byte 8 - Set to Ø (Reserved)

Byte 9 - Set to Ø (Reserved)

SECTION 4

MAINTENANCE AND TROUBLESHOOTING

4.1 Overview

Three maintenance and troubleshooting aids are provided with the Controller: Sense Byte Error Codes, Class Code 7 Commands, and Controller mounted LED's.

The Sense Byte Error Codes (given in Table 3-2) are provided with the Class Code Ø OpCode Ø3 (Request Sense Bytes) Command. The Sense Byte Error Codes, described in Paragraph 3.2.4, define an error as:

Type Ø - Drive Related
Type 1 - Controller Related
Type 2 - Command Related
Type 3 - Miscellaneous

This section describes the Class Code 7 commands and the 8 LED's (Light Emitting Diodes) mounted on the Controller.

4.2 Class Code 7 Commands

Class Code 7 commands are diagnostic commands described in Section 5, Maintenance and Troubleshooting.

Class Code 7 commands are issued with a standard Command Descriptor Block (CDB). The valid CDB for each OpCode is shown in this section. See Sections 2 and 3 of this manual for additional information on CDB's and commands.

Table 4-1 is a summary of the Class Code 7 OpCodes.

TABLE 4-1

Class Code 7 OpCodes

OpCode Hex)	Command Description
ØØ	RAM diagnostics - Performs test on RAM
Ø1	Write ECC Command - This OpCode writes data on the disk that is displaced by three bytes. Data written with this command code allows programming control for writing the ECC character.
Ø2	Read ID Field - Transfers only the ID Field (Cylinder Head, Sector, and their 3 ECC Check Characters) from the specified Logical Address.(Not valid for floppy)
Ø3	Perform Drive Diagnostic Ø - Causes a sequential read of all Sector Ø's, and then a read of 256 randomly selected Sector Ø's.
Ø6	Request Logout - Returns four bytes of error information from the specified LUN to the Host. Each LUN has its own error log which is set to zero after each Request Logout Command

4.2.1 OpCode ØØ (RAM Diagnostics).

A diagnostic test is performed on the Controller RAM storage upon application of power and when this command is executed.

	MSB							LSB
BYTE #	7	6	5	4	3	2	1	Ø
Ø	1	1	1	Ø	Ø	Ø	Ø	1
1	LUN			LAD 2				
2	LAD 1							
3	LAD Ø							
4	Set to Ø							
5	Set to Ø							

4.2.2 OpCode Ø1 (Write ECC Error Command) (not valid for floppy)

This command writes a block of data on the disk without generating a readable ECC for the data. This OpCode writes data on the disk that is displaced by three bytes. Data written with this command code will give an invalid ECC error when it is read. The ECC error circuitry is checked when data written with this OpCode is read.

The required CDB fields for this command are OPCODE, LUN, LAD 2, LAD 1, and LAD Ø.

	MSB							LSB
BYTE #	7	6	5	4	3	2	1	Ø
Ø	1	1	1	Ø	Ø	Ø	Ø	1
1	LUN			LAD 2				
2	LAD 1							
3	LAD Ø							
4	Set to Ø							
5	Set to Ø							

See the Flowchart in Figure 4-1 for additional information.

Class 7
OpCode = 1

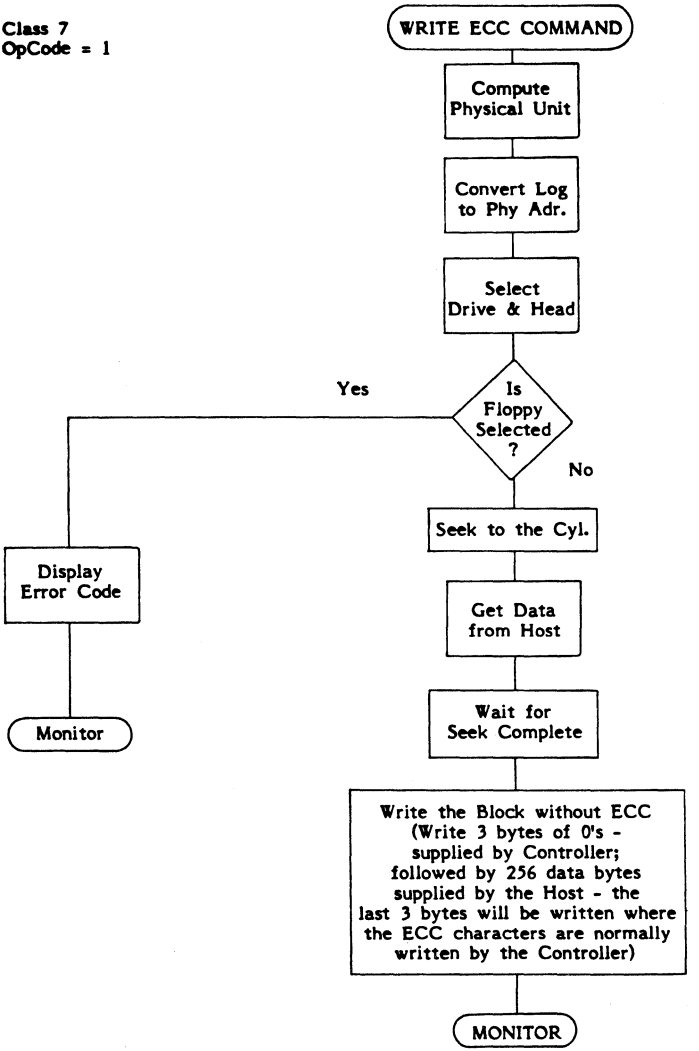


Figure 4-1 Write ECC Command

4.2.3 OpCode Ø2 (Read ID Field) (not valid for floppy)

This command reads the ID field in the sector specified by the LAD, and transfers them to the Host as data (C/D deasserted).

The required CDB bytes for this command are: OPCODE, LUN, LAD 2, LAD 1, LAD Ø, and INTERLEAVE CODE.

	MSB							LSB
BYTE #	7	6	5	4	3	2	1	Ø
Ø	1	1	1	Ø	Ø	Ø	1	Ø
1	LUN			LAD 2				
2	LAD 1							
3	LAD Ø							
4	INTERLEAVE CODE							
5	Set to Ø							

See the flowchart in Figure 4-2 for additional information.

Class 7
OpCode = 2

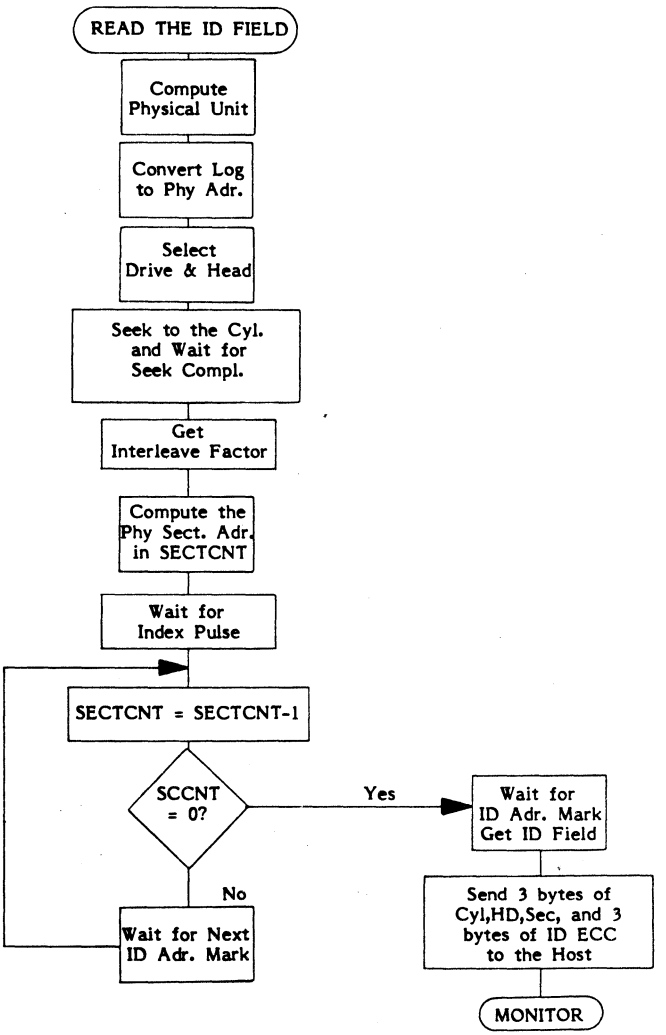


Figure 4-2 Read ID Field

4.2.4 OpCode Ø3 (Perform Drive Diagnostic)

This command performs a diagnostic test on the LUN specified. It will cause a sequential read of Sector Ø on all tracks (from track Ø to the specified maximum track) and will then read Sector Ø on 256 randomly selected tracks.

The required CDB bytes for this command are: OPCODE and LUN.

	MSB							LSB
BYTE #	7	6	5	4	3	2	1	Ø
Ø	1	1	1	Ø	Ø	Ø	1	1
1	LUN					Ø		
2	Ø							
3	Ø							
4	Ø							
5	Ø							

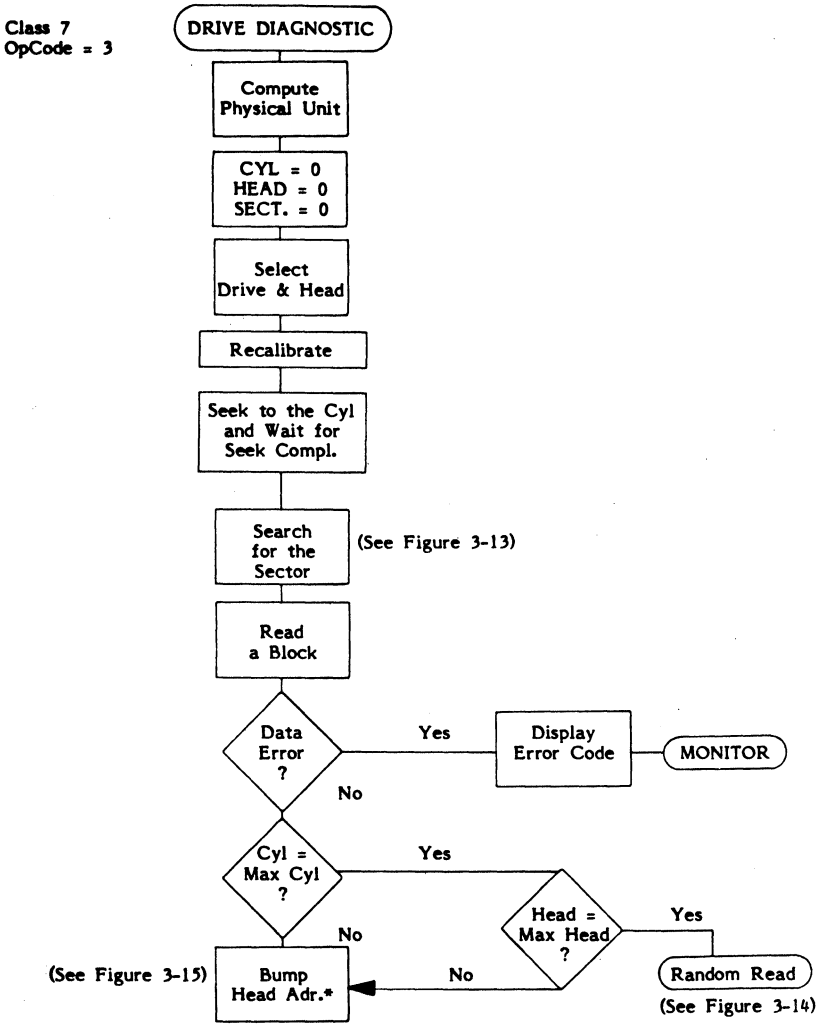
See the flowchart in Figure 4-3 for additional information.

4.2.5 OpCode Ø6 (Request Logout)

This command is used to retrieve four bytes of error log information for the LUN specified in the CDB. Each device has its own error log area which accumulates the errors made by that device. This error log area is cleared when error information on the device is transferred.

The required CDB bytes for this command are: OPCODE and LUN.

	MSB							LSB
BYTE #	7	6	5	4	3	2	1	Ø
Ø	1	1	1	Ø	Ø	1	1	Ø
1	LUN					Ø		
2	Ø							
3	Ø							
4	Ø							
5	Ø							



* Refer to INHD Routine (Bump Head Adr.)

Figure 4-3 Drive Diagnostic Command

4.2.5 OpCode Ø6 (Request Logout) (continued)

The following errors are accumulated in the error log area:

Correctable data error
Uncorrectable read error in the ID field
Uncorrectable read error in the Data field
No ID field Address Mark
Seek Error Condition
No Record Found Condition

The format of the error log area is:

	MSB							LSB
BYTE #	7	6	5	4	3	2	1	Ø
Ø	Retry Count - High Order Bits							
1	Retry Count - Low Order Bits							
2	Permanent Error - High Order Bits							
3	Permanent Error - Low Order Bits							

Byte Ø contains the upper 8 bits for the total number of errors detected, excludes I/D field errors which are not retried (i.e., retry attempts are counted).

Byte 1 contains the lower 8 bits for the total number of errors detected, excludes I.D field errors which are not retried (i.e., retry attempts are counted).

Byte 2 contains the upper 8 bits for the total number of hard read errors plus the I/D field errors that have occurred (i.e., all unsuccessful retry attempts and I/D field errors are counted)

Byte 3 contains the lower 8 bits for the number of hard read errors plus the I/D field errors that have occurred (i.e., all unsuccessful retry attempts and I/D field errors are counted).

4.3 LED Error Display

The Controller has 8 Light Emitting Diode (LED) indicators. If an error should occur it is presented to the interface in the Status byte (as described in Section 3) saved in the error log area, and a hexidecimal value is placed in the 8 LED's. The value in the LED's is reset when any subsequent command is issued.

Table 4-2 lists the error indication for each hexidecimal value displayed with these LED's. The LED's will display 40 Hex when the Controller is idling and monitoring its interface; and C0 Hex when the Controller is selected.

TABLE 4-2

LED ERROR DISPLAY

Lit LED indicated by a 1

Hex Error Code	DS8							DS1	Description
ØØ	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	No error condition, normal operation
Ø1	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	No Index pulse from drive
Ø2	Ø	Ø	Ø	Ø	Ø	Ø	1	Ø	No Track ØØ from drive after recal
Ø3	Ø	Ø	Ø	Ø	Ø	Ø	1	1	Sector Address beyond maximum
Ø4	Ø	Ø	Ø	Ø	Ø	1	Ø	Ø	Winchester drive not selected
Ø5	Ø	Ø	Ø	Ø	Ø	1	Ø	1	No Seek Complete from drive
Ø6	Ø	Ø	Ø	Ø	Ø	1	1	Ø	No ID Address Mark received
Ø7	Ø	Ø	Ø	Ø	Ø	1	1	1	No Data Address Mark receieved
Ø8	Ø	Ø	Ø	Ø	1	Ø	Ø	Ø	Seek Error, Cylinder or Head wrong
Ø9	Ø	Ø	Ø	Ø	1	Ø	Ø	1	Sector not found
ØA	Ø	Ø	Ø	Ø	1	Ø	1	Ø	ECC error in ID field
ØC	Ø	Ø	Ø	Ø	1	1	Ø	Ø	Invalid Command received
ØD	Ø	Ø	Ø	Ø	1	1	Ø	1	Incorrect Data Mark
ØE	Ø	Ø	Ø	Ø	1	1	1	Ø	Incorrect ID Mark
ØF	Ø	Ø	Ø	Ø	1	1	1	1	Incorrect Cylinder Address from drive
1Ø	Ø	Ø	Ø	1	Ø	Ø	Ø	Ø	Incorrect Sector Addrress from drive
11	Ø	Ø	Ø	1	Ø	Ø	Ø	1	Incorrect Head Address from drive
12	Ø	Ø	Ø	1	Ø	Ø	1	Ø	Uncorrrectable Data Error
13	Ø	Ø	Ø	1	Ø	Ø	1	Ø	Correctable Data Error
14	Ø	Ø	Ø	1	Ø	1	Ø	Ø	Drive not Ready
15	Ø	Ø	Ø	1	Ø	1	Ø	1	Write Fault Condition
17	Ø	Ø	Ø	1	Ø	1	1	1	Drive is Write Protected
18	Ø	Ø	Ø	1	1	Ø	Ø	Ø	RAM diagnostic error
1F	Ø	Ø	Ø	1	1	1	1	1	Unable to read Alternate Track
2Ø	Ø	Ø	1	Ø	Ø	Ø	Ø	Ø	Host Adapter has Parity circuit fault
21	Ø	Ø	1	Ø	Ø	Ø	Ø	1	Bad Block detected from drive
22	Ø	Ø	1	Ø	Ø	Ø	1	Ø	Invalid function for drive type
31	Ø	Ø	1	1	Ø	Ø	Ø	1	Attempted to directly access an alternate Track
32	Ø	Ø	1	1	Ø	Ø	1	Ø	Seek in process
33	Ø	Ø	1	1	Ø	Ø	1	1	Volume overflow
4Ø	Ø	1	Ø	Ø	Ø	Ø	Ø	Ø	Idle condition
81	1	Ø	Ø	Ø	Ø	Ø	Ø	1	Mutliple LUN's selected, fatal error
82	1	Ø	Ø	Ø	Ø	Ø	1	Ø	Sequence time-out during disk transfers
CØ	1	1	Ø	Ø	Ø	Ø	Ø	Ø	Controller Selected

NOTE: Values not shown are unused.

4.4 Troubleshooting

The indications given by the LED's and the Sense Byte are detailed to simplify the isolation of any fault that may occur.

SECTION 5

APPENDICES - INSTALLATION AND GENERAL INFORMATION

5.1 Introduction

The following Appendices contain general information, jumper and switch settings, and board layout diagrams for the DTC 500B Series Controllers.

5.2 Mounting

There are no special mounting requirements. The Appendices provide the location of the mounting holes. The provided mounting holes are compatible to those used with industry standard 5.25" drives. (to facilitate mounting the Controller on the drives).

Up to eight (8) controllers can be daisy chained on the SASI Bus. Only the controller that is physically at the end of the daisy chain should have the terminator resistors installed.

The temperature specifications given in Table 1-2 must be maintained to ensure reliability standards.

APPENDIX A

LOGICAL ADDRESS

A.1 Overview

Logical Address is an accumulation of the number of Sectors, for each head, at each cylinder.

For example:

If the drive (designated by the LUN) has 16 Sectors per track (Ø through 15) and 2 heads (Ø and 1).

Cylinder Ø, Head Ø would contain Logical Address ØØØ through Ø15, and Head 1 would contain Logical Addrress Ø16 through Ø31.

Cylinder 1, Head Ø would contain Logical Address Ø32 through Ø47, and Head 1 would contain Logical Addrress Ø48 through Ø63,etc. The highest possible Logical Address is assigned to the 16th Sector of Head 1, at the maximum allowable Cylinder Address.

The Logical Address concept is an attempt to enable software to be written which is device independent. This is accomplished by using the selected drive's parameters (such as the highest possible cylinder address, number of sectors per track) when calculating the Logical Address.

When the selected drive is changed (a new LUN) the parameters can be changed if required. The formula (used to calculate the Logical Address) determines the new Logical Addresses assigned to each Sector within the drive.

A.2 Calculation of Logical Address

Each Logical Address is calculated by multiplying the cylinder address, by the number of heads per cylinder, then multiplying this result by the number of sectors per track, and then adding this result. The results obtained by multiplying the number of sectors by the head address; to this value the sector address is added.

The formula for this calculation is:

$$LA = ((C) (h) (s)) + ((H) (s) + (S))$$

Where LA = Logical Address
C = Cylinder Address
h = Number of heads per cylinder
s = Number of sectors per track
H = Head Address
S = Sector Address

A.2 Calculation of Logical Address (continued)

With this formula a unique Logical Address for each Sector on any drive can be established.

For example:

Assume LUN Ø is a drive with a maximum Cylinder Address of 256 (Ø to 255) that has 4 heads per cylinder (head addresses of Ø to 3), and 33 sectors per track (sector addresses of Ø to 32). The highest Logical Address for this drive would be calculated as follows:

((255) (4) (33)) + ((3) (33)) + 32 = Logical Address

or

33,66Ø + 99 + 32 = 33,791

which is the highest Logical Address for this drive.

Another way to visualize the formula is to recognize that the Logical Address is being incremented by a value of 1 each sector during a format of the drive.

In the above example, each head at cylinder Ø would advance the Logical Address by 33, and the Logical Address, at cylinder Ø, Sector Address 32 (the 33rd sector), Head 3 (the 4th head) would be 131 (4 times 33 less 1 because of starting at Ø).

Each cylinder increment would advance the Logical Address an equivalent amount (132) and since there are 256 cylinders the largest Logical Address is 132 x 256 = 33,792 - 1 (because of Ø) or 33,791.

A.3 Determining Cylinder Addresses

One method of determining the cylinder address from the Logical Address is to divide the Logical Address value by the result obtained by multiplying the number heads per cylinder by the number of sectors per track.

The results of this calculation will be a whole number and a fraction. The whole number is the Cylinder Address, the fraction is explained on the following page.

(LA / h x s) = Cylinder Address and fraction

Where LA = Logical Address
h = heads per cylinder
s = sectors per track
/ = indicates divide and x indicates multiply

The fraction is a function of the number of heads. In our example (with 4 heads):

A fraction between .ØØ1 and .25Ø indicates head Ø, .251 to .5ØØ indicates head 1, .5Ø1 to .75Ø indicates head 2, and .751 to .999 indicates head 3.

If we had chosen an example using 2 heads, a value of .5Ø or less would indicate head Ø and a value of .51 or greater would indicate head 1.

APPENDIX B

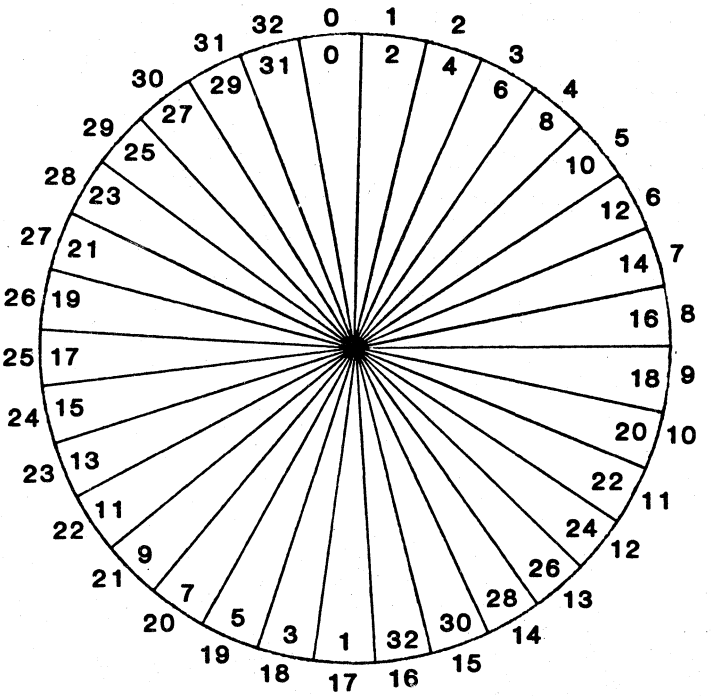
INTERLEAVE

B.1 Interleave

Interleaving is a process which assigns a Logical Sector Address to each Sector that differs from its Physical Address. The purpose is to allow the Host time to manipulate the data received from a Sector and be able to get the next required Sector of information from the disk without having to wait for a full revolution of the disk.

The Interleave factor is assigned by byte 4 in Class Code Ø CDB's with a Format Drive, Format Track, Format Bad Track, Check Track Format, Read ID and assign alternate Track OpCodes.

A representation of Physical Sector versus Logical Sector, with a 33 Sector format and an interleave factor of 2 and 6, is shown in Figure B-1.

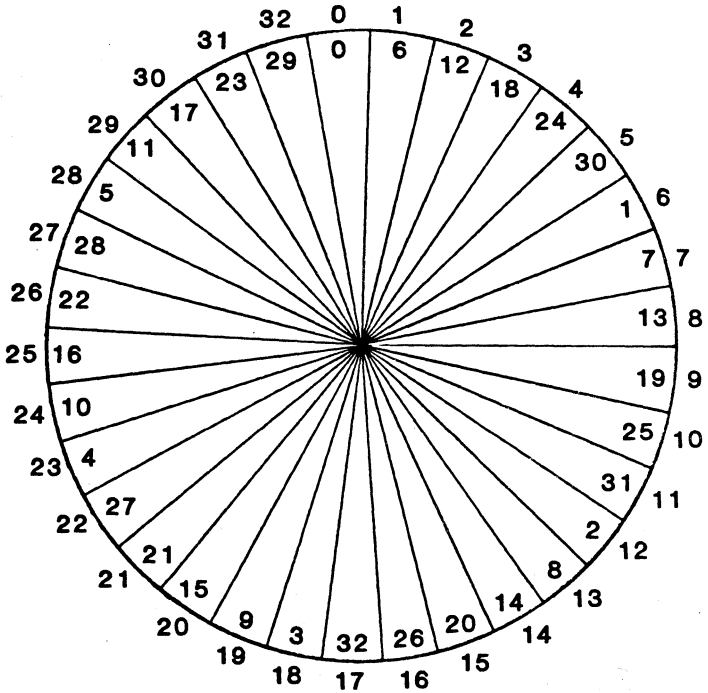


PHYSICAL SECTOR NUMBER IS OUTER NUMBER.

LOGICAL SECTOR NUMBER IS INNER NUMBER.

FIGURE B-1 PHYSICAL VERSUS LOGICAL SECTOR (SHEET 1 OF 2)

INTERLEAVE FACTOR = 2



PHYSICAL SECTOR NUMBER IS OUTER NUMBER.

LOGICAL SECTOR NUMBER IS INNER NUMBER.

FIGURE B-1 PHYSICAL VERSUS LOGICAL SECTOR (SHEET 2 OF 2)

INTERLEAVE FACTOR = 6

APPENDIX C

SECTOR FORMATS

C.1 Winchester Drive Sector Formats

This paragraph describes the available Winchester drive formats.

C.1.1 256 Bytes per Sector/33 Sectors per Track

The track layout for 256 bytes per sector/33 sectors per track is shown below:

13 bytes ØØ's	am	FE	ID Ø	ID 1	ID 2	ecc	Ø	Ø	13 bytes ØØ's	am	F8	256 bytes data	ecc	Ø	Ø	1Ø bytes 4E's

am, FE, IDØ, ID1, ID2, ØØ, F8 = 1 byte
ecc = 3 bytes

Track Capacity = 1Ø,416

16	=	Index Gap (4E)
1Ø,197	=	33 sectors @ 3Ø9 bytes/sector
2Ø3	=	Speed Tolerance Gap (4E)
1Ø,416		

3Ø9 bytes/sector including ID and overhead

This track format provides (+ or -) 1.77% speed tolerance.

C.1.2 512 Bytes per Sector/18 Sectors per Track

The track layout for 512 bytes per sector/18 sectors per track is shown below:

13 bytes ØØ's	am	FE	ID Ø	ID 1	ID 2	ecc	Ø	Ø	13 bytes ØØ's	am	F8	512 bytes data	ecc	Ø	Ø	14 bytes 4E's

am, FE, IDØ, ID1, ID2, ØØ, F8 = 1 byte
ecc = 3 bytes

```
Track Capacity =  1Ø,416
                     16  =  Index Gap (4E)
                  1Ø,242  =  18 sectors @ 569 bytes/sector
                     158  =  Speed Tolerance Gap (4E)
                  1Ø,416
```

569 bytes/sector including ID and overhead

This track format provides (+ or -) 1.29% speed tolerance.

C.1.3 1,Ø24 Bytes per Sector/9 Sectors per Track

The track layout for 1,Ø24 bytes per sector/9 sectors per track is shown below:

13 bytes ØØ's	am	FE	ID Ø	ID 1	ID 2	ecc	Ø	Ø	13 bytes ØØ's	am	F8	1,Ø24 bytes data	ecc	Ø	Ø	58 bytes 4E's

am, FE, IDØ, ID1, ID2, ØØ, F8 = 1 byte
ecc = 3 bytes

```
Track Capacity =  1Ø,416

                     16  =  Index Gap (4E)
                  1Ø,242  =  9 sectors @ 1,125 bytes/sector
                     275  =  Speed Tolerance Gap (4E)
                  1Ø,416
```

1,125 bytes/sector including ID and overhead

This track format provides (+ or -) 2.50% speed tolerance.

C.2 Floppy Drive Formats

FM recording utilizes the IBM 1D format.
MFM recording utilizes the IBM 2D format.

APPENDIX D

ALTERNATE TRACK USAGE WITH DTC CONTROLLERS

Alternate Tracks are used to replace the bad tracks found during system initialization so that the Host system will have a continuous range of disk memory with no defects. The preferred scheme is to place all the alternate tracks at the top of the disk memory, (i.e., the inner track), so that the Host system can simply map out these tracks and reduce the maximum logical address that the Host system is allowed to access on the disk. Following this scheme, a sample procedure for assigning alternate tracks might be as follows:

1. Initalize Controller with the appropriate drive characteristics. (All cylinders and heads must specified).

2. Format the entire drive and verify the disk.

3. Assign an alternate for each defective track making sure that no two defective tracks are assigned to the same alternate.

4. Consider assigning alternates for tracks on the drive manufacturer's list of defects.

5. Accumulate the number of tracks taken by the alternates and map them out from the range of disk memory which the Host system is allowed to access on the disk (i.e., if the top two tracks are used for alternates, the maximum track address that the system should access directly is two less than the amount specified in the Define Drive Parameter Command).

6. Repeat steps 1 through 5 if more than one Winchester drive is to be implemented.

Future accesses to those *defective tracks will result in accessing the corresponding alternates and will be transparent to the Host system.

APPENDIX E

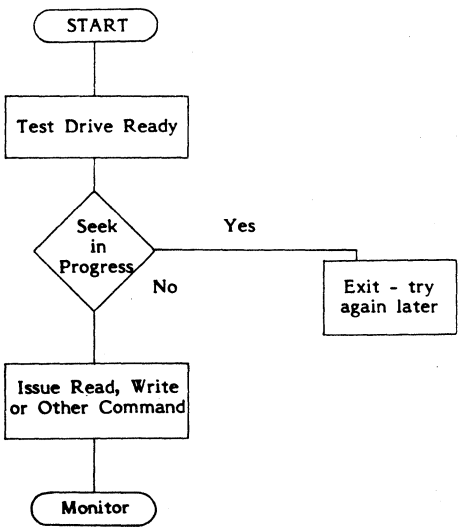
IMPLEMENTING OVERLAPPED SEEKS ON DTC DISK CONTROLLERS

For Winchester drives capable of performing overlapped seeks, the overlap function can be utilized by setting a bit in the drive parameters while issuing the Class 6 OpCode 2 command. When the DTC disk Controller receives a seek command it issues the required step pulses which the drive buffers. The Controller then checks a bit in the internal drive characteristic table and if the overlapped function is allowed, it returns the completion status to the Host without waiting for the seek complete condition from the drive.

A typical implementation of this function might be where the Host issues an overlapped seek to drive "A" and while the drive is seeking, the Host could perform other tasks which includes servicing or initiating yet another task on other drives.

If Test Drive Ready command is received for the drive while the drive is still seeking, the Controller will respond with an error Type Ø Code D, seek in progress. The Host can decide to perform some other task or keep issuing the command until a normal termination is received, signifying a successful completion of the command.

This mode cannot be used on drives like the ST5Ø6 that cannot support overlap seek operation. The Controller will deselect the drive after the step pulses have been sent to the drive.



APPENDIX F

JUMPER SETTINGS FOR 510B

Parity

The jumper between 4C and 5C labeled PARITY is to enable parity reception.
Parity is always enabled as an output.

SECTOR SIZE

Sector Size Jumpers (located between 7F and 7E)

SECT512	SECT1024	Sector Size
out	out	256
in	out	512
out	in	1024
in	in	1024

CONTROLLER ID SELECTION

Controller ID jumpers are located between IC's 7E and 8E. One Shunt specifies the Controller's ID address.

FACTORY SETTINGS:

PARITY - IN
ID - ID0

SECTOR SIZE JUMPERS

512	IN
1024	OUT

Termination resistor packs are located at 3F and RP1.

Figure F-1 DTC-510B Cable Connectors

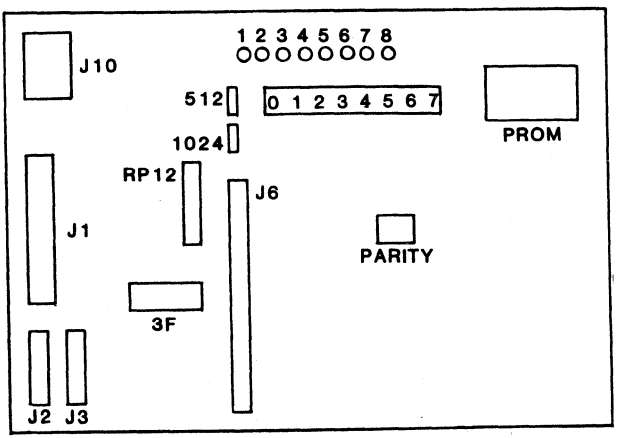
J1 - 34 pin connector: Connects Winchester Drive's Control Interface to Controller. See Figure 2-3 for pin designations.

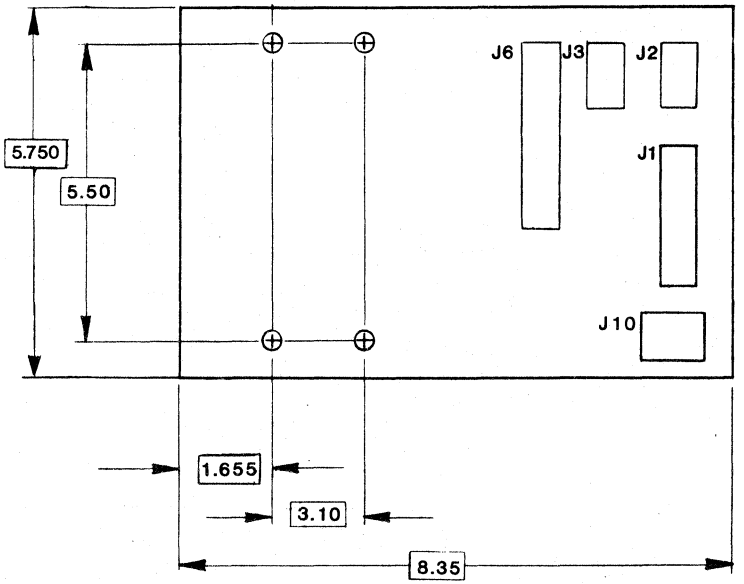
J2,J3 - 20 pin connector: Connects Winchester Drive's Data Interface to Controller. See Figure 2-4 for pin designations.

J6 - 50 pin connector: Connects the Host to the Controller. See Figure 2-2 for pin designations.

J10 - 4 pin connector: AMP - 1-48042-1 for connector, AMP- 350078-4 for pins (or equivalent), connects D.C. Power to Controller. Pin assignment is as shown below:

Pin 1 - No connection
Pin 2 - Ground
Pin 3 - Ground
Pin 4 - +5 vDC, 2.6 Amps





ALL DIMENSIONS ARE INCHES

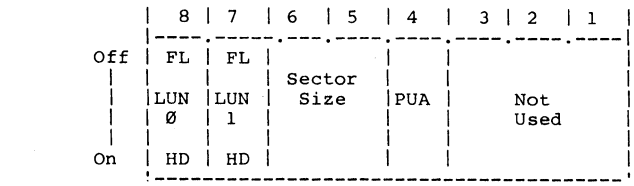
NOT DRAWN TO SCALE

Figure F-2 DTC 510B Board Dimensions with Mounting Holes

APPENDIX G

SWITCH SETTINGS AND JUMPER CONFIGURATIONS FOR 52ØB

Switches (location 2E)



FL = Floppy
HD = Hard Disk
PUA= Power Up Alert
LUN 2 and 3 are always floppies.

Power Up Alert Switch

Switch 4 is used to detect power up alert. If the switch is on, the Controller will abort the first command after power up/reset and set bit 2 of the completion status byte to 1.

- Sector Size Control - Switches 6 and 5

Select Switches 6	5	Sector Size.
on	on	Not Used
on	off	1Ø24 Bytes
off	on	512 Bytes
off	off	256 Bytes

- PARITY SELECT JUMPER (Location X2 near 7C)

In - Parity Enabled

Out - Parity Disabled

CONTROLLER ID SELECTION

Controller ID jumpers (J4) are located near the Host Connector J6. One shunt specifies the Controller ID address.

Termination resistor packs are located at 2H and PR4.

Figure G-1 DTC-520B Cable Connectors

J1 - 34 pin connector: Connects Winchester Drive's Control Interface to Controller. See Figure 2-3 for pin designations.

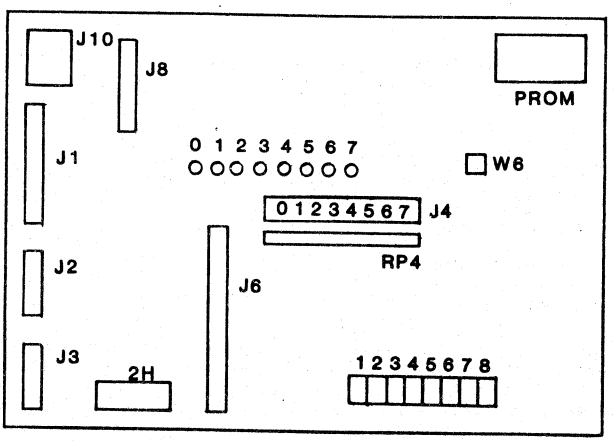
J2,J3 - 20 pin connector: Connects Winchester Drive's Data Interface to Controller. See Figure 2-4 for pin designations.

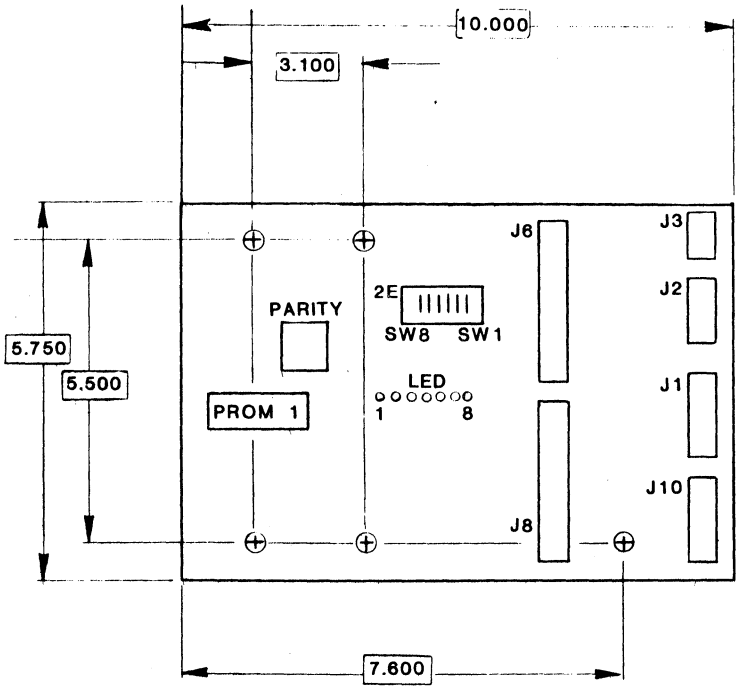
J6 - 50 pin connector: Connects the Host to the Controller. See Figure 2-2 for pin designations.

J8 - 34 pin connector: Connects Floppy drives to Controller. See Figure 2-5 for pin designations.

J10 - 4 pin connector: AMP - 1-480424-0 for connector, AMP- 350078-4 for pins (or equivalent), connects D.C. Power to Controller. Pin assignment is as shown below:

Pin 1 - No connection
Pin 2 - Ground
Pin 3 - Ground
Pin 4 - +5 vDC, 3.4 Amps





ALL DIMENSIONS ARE INCHES
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NOTE: IF PARITY JUMPER (NEAR 7C) IS IN, THE PARITY IS ENABLED

Figure G-2 DTC 520B Board Dimensions with Mounting Holes

APPENDIX H

SWITCH SETTINGS FOR 535B

Switches 7 and 8 determine the configuration of LUN's 2 and 3. LUN's Ø and 1 are always a hard disk.

SWITCH 8	SWITCH 7	
ON	ON	LUN's 2 and 3 are both AMLYN Drives.
ON	OFF	LUN 2 is an AMLYN Drive. LUN 3 is an 8 inch Floppy Drive.
OFF	XX	LUN's 2 and 3 are both 8 inch Floppy Drives.

Sector Size Control:

Switch 6	Switch 5	Winchester Track Format
OFF	OFF	256 Byte/ Sector 33 Sectors
OFF	ON	512 Bytes/ Sector 18 Sectors
ON	OFF	1Ø24 Bytes/ Sector 9 Sectors
ON	ON	Not Used

Switch 4 - If the switch is on, the Controller will abort the first command after power up/reset and set bit 2 of the completion status byte to 1.

Controller ID Selection:

Switch 3	Switch 2	Switch 1	ID Number
On	On	On	Ø
On	On	Off	1
On	Off	On	2
On	Off	Off	3
Off	On	On	4
Off	On	Off	5
Off	Off	On	6
Off	Off	Off	7

Termination resistor packs are located at RP13 and RP14.

APPENDIX H (continued)

Figure H-1 DTC-535B Cable Connectors

J1 - 34 pin connector: Connects Winchester Drive's Control Interface to Controller. See Figure 2-3 for pin designations.

J2,J3 - 20 pin connector: Connects Winchester Drive's Data Interface to Controller. See Figure 2-4 for pin designations.

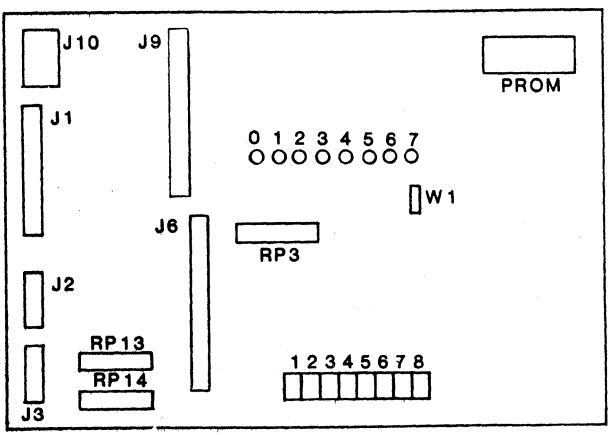
J6 - 50 pin connector: Connects the Host to the Controller. See Figure 2-2 for pin designations.

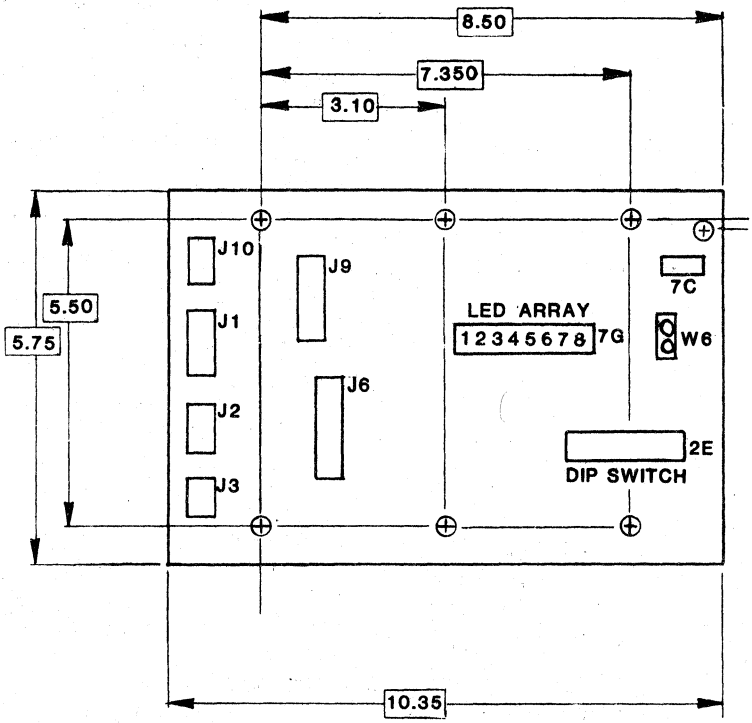
J9 - 50 pin connector: Connects Floppy drives to Controller. See Figure 2-7 for pin designations.

J10 - 4 pin connector: AMP - 1-480424-0 for connector, AMP- 350078-4 for pins (or equivalent), connects D.C. Power to Controller. Pin assignment is as shown below:

Pin 1 - No connection
Pin 2 - Ground
Pin 3 - Ground
Pin 4 - +5 vDC, 3.4 Amps

Jumper W1 = Jumpered A to B indicates odd parity.





ALL DIMENSIONS ARE INCHES

NOT DRAWN TO SCALE

Figure H-2 DTC 535B Board Dimensions with Mounting Holes

APPENDIX H-1 JUMPER SETTINGS FOR SA800/801

The following information is contained in the SA800/801 Diskette Storage Drive OEM Manual, Shugart Associates, 1977.

Jumper Name	Function (Enabled if Jumper installed)
A	Enable DRSEL to drive selection
B	Installed, Head Load on Unit Select
C	Removed, Unit Select loads heads
D	Remove, In Use to led is disabled
DC	Removed, Disable Disk Change to return to Controller.
DS	Enable stepper on USel
DS1-4	Drive Select; one only; set for LUN
HL	Removed, Head load on Unit Select
L	Jumper for -5V(remove for -15V).
T1	Remove, Head Load terminator
T2	Install, Pullup for DSx
T3	Install, Direction terminator
T4	Install, Step terminator
T5	Install, Wr Data terminator
T6	Install, Wr Gate " "
X	Install, Head Load Enable
Y	Removed, Disable Hdld from driving led
Z	USel drives in use led
800	Install, enables 800 index only operation
801	Removed, disables 801 mode operation

APPENDIX H-2 JUMPER SETTINGS FOR SA850/SA851 FLOPPY

Jumper Name	Function (Enabled if Jumper installed)
DS1-4	Drive Select
FS	In
IT	In
IW	In
RS	In
S2	In
-5	In
850	In

All other jumpers Out.

APPENDIX H-3 JUMPER SETTING FOR TANDON TA848-1/2

Jumper Name	Function (Enabled if Jumper installed)	
DS1-4	Drive Select; one only; set for LUN	
S2-S3	In	Side Select TM848-2 only
S1-S3	Out	Side Select from Drive Sel
HLL	Out	Head Load F-F
C	Out	Head Load Line
DS	Out	Drive always selected
M1	In	Motor On with Drive Sel
M2	Out	Motor On with Motor off control

APPENDIX H-4 JUMPER SETTINGS FOR AMLYN 585Ø

JUMPER CONFIGURATION FOR THE AMLYN 585Ø

1. H JUMPER - jumpered: drive always selected.
   C JUMPER - open: Unit Select Ø.
   D JUMPER - open: Unit Select 1.
   E JUMPER - open: Unit Select 2.
   F JUMPER - open: Unit Select 3.

2. AH JUMPER - open: Binary Address mode - Drive Ø.

3. AK JUMPER - open: disable Side Select Enable.

4. AJ JUMPER - shunt: enable Head Load

5. W JUMPER - jumpered: Drive ready.
   AA JUMPER - jumpered: Drive ready.

6. AL JUMPER - jumpered: Write Protect Enable.
   AC JUMPER - jumpered: Write Protect Enable.

7. AB JUMPER - jumpered: In use LED.

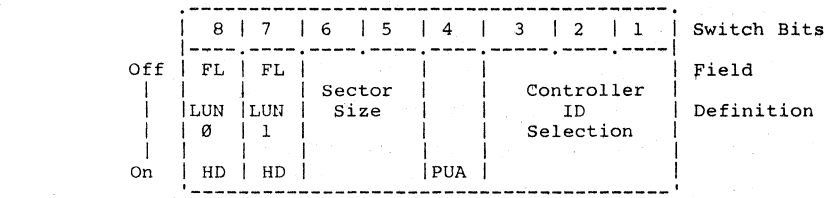
8. Y JUMPER - short: (near R2) single actuator mode

9. M JUMPER- open: disable Self Exercise Mode.

APPENDIX J

SWTICH SETTINGS FOR 535BK CONTROLLER

INTERNAL SWITCHES (location 2E)



FL = Floppy
HD = Hard Disk

PUA = Power Up Alert
LUN 2 and 3 are for floppies only.

POWER UP ALERT

Switch 4 - If switch is on, the Controller will abort the first command after power up/reset and set bit 2 of the completion status byte to 1

SECTOR SIZE CONTROL - Switches 6 and 5

Select Switches 6	5	Sector Size.
on	on	Not Used
on	off	1024 Bytes
off	on	512 Bytes
off	off	256 Bytes

Controller ID Selection:

Switch 3	Switch 2	Switch 1	ID Number
On	On	On	0
On	On	Off	1
On	Off	On	2
On	Off	Off	3
Off	On	On	4
Off	On	Off	5
Off	Off	On	6
Off	Off	Off	7

JUMPER CONFIGURATION GUIDE FOR 535BK

Jumper Configuration Guide

PARITY ENABLE (Location W6 near IC 7C)

IN - Receive Parity Check Enable: Parity enabled.

OUT - Receive Parity Check Disable: Parity disabled.

NOTE: The DTC 535BK Generates Odd Parity in either position.

External Power Reset (Location W1 near J1Ø).

IN - Enables Pin 2 of the Power Connector (J1Ø) to reset the board when Low.

OUT - This function is disabled.

Termination resistor packs are located at 2H and RP4.

APPENDIX J (continued)

J-1 DTC-535BK Factory Settings (jumpers as shipped from DTC)

W1	OUT
W2	Center to right
W6	IN (shunt)
W7	IN (wired) (Kodak connection)

Enhanced ECC Jumpers (for enabling use of PØ37 or P134)

JUMPER or IC	PØ37	P134 @ IC position 5A
W3	OUT	IN
W4	OUT	IN
W5	Center to right	Center to left
IC 5B FB8VA	IN	OUT
IC 4D 7416	IN	OUT
Resistor R38 (1K)	IN	OUT (near 4B)

J-2 SWITCH SETTINGS FOR KODAK 3.3 SUPER MINIFLOPPY

Switch Name	Function (Selected if switch on)
1	Drive Select 1
2	Drive Select 2
3	Drive Select 3
4	Drive Select 4

Important: In order for the drive to function properly, the HL jumper (head load option) on the drive PCB must be cut. This will eliminate the time it takes for the heads to load and unload during a disk copy. Refer to your drive manual for further details on this option.

Figure J-1 DTC-535BK Cable Connectors

J1 - 34 pin connector: Connects Winchester Drive's Control Interface to Controller. See Figure 2-3 for pin designations.

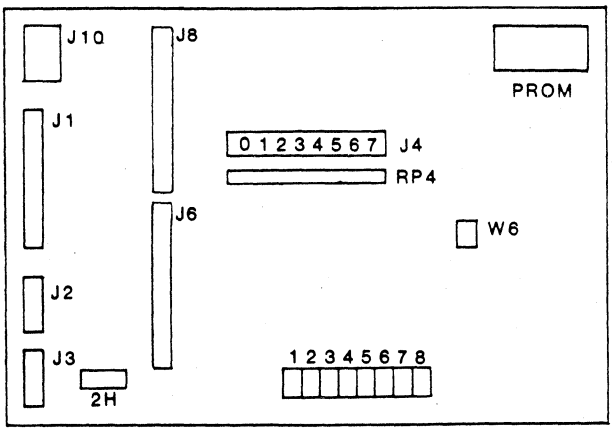
J2,J3 - 20 pin connector: Connects Winchester Drive's Data Interface to Controller. See Figure 2-4 for pin designations.

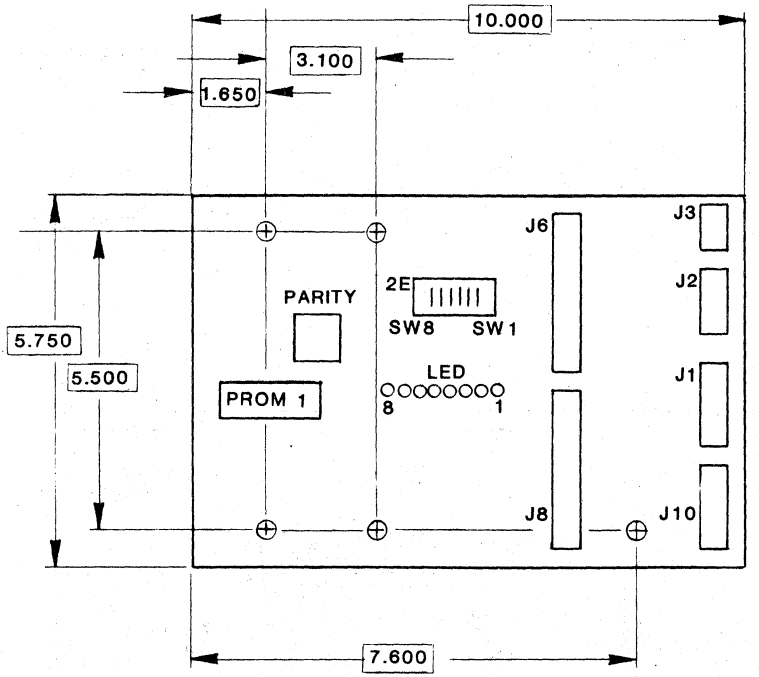
J6 - 50 pin connector: Connects the Host to the Controller. See Figure 2-2 for pin designations.

J8 - 34 pin connector: Connects Kodak Drive's Controller. See Figure 2-8 for pin designations.

J10 - 4 pin connector: AMP - 1-480424-0 for connector, AMP- 350078-4 for pins (or equivalent), connects D.C. Power to Controller. Pin assignment is as shown below:

Pin 1 - No connection
Pin 2 - Ground
Pin 3 - Ground
Pin 4 - +5 vDC, 3.4 Amps





ALL DIMENSIONS ARE INCHES

NOT DRAWN TO SCALE

Figure J-2 DTC 535BK Board Dimensions with Mounting Holes


DTC